



WBS 6.8

Trigger

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U.S. ATLAS HL-LHC Conceptual Design Review
Technical Session
Arlington, VA
Mar 8-10, 2016



Biography

- Elliot Lipeles

- Associate Professor at University of Pennsylvania
- Lead ATLAS Trigger “menu” group from (2012-2013)
 - menu = list of threshold used
 - a key step in the performance requirements
- Long-term activity in ATLAS Trigger architecture
 - One of initial advocates planned system architecture
 - Editor of architecture chapter of ATLAS internal review of the initial design
- Actively involved in simulation of HL-LHC trigger system
- ATLAS Trigger Rate group leader 2008-2014
- Analysis Higgs to WW, Higgs to Invisible, Standard Model Dibosons, SUSY trileptons, SUSY stop squark
- Other experience: CMS DAQ/HLT installation coordination, CDF Offline computing farm management, CLEO DAQ hardware and data-handling and control software



Outline

- Trigger Intro (people, groups,...)
- Physics Requirements and Flow down to performance and technical requirements
 - Scope of ATLAS HL-LHC Trigger Upgrade
 - Scope of NSF supported Deliverables
 - Integration, Milestones, Risk, ...
 - R&D efforts
- Closing Remarks



Trigger System Overview

- The Trigger system is an online data selection system
 - Reduces data to be readout to a technically feasible volume
 - 40 MHz beam crossing rate to planned 400 kHz readout rate
 - For the 5 MB raw event size, that means a reduction from 200 TB/s to 2 TB/s
 - Reduces data volume to be stored for offline analysis
 - 400 kHz (200 PB/day) readout rate to 10 kHz (5 PB/day) storage rate
 - The selections implemented in the trigger have a strong role in defining the physics performance of the experiment
- The Trigger and DAQ group in ATLAS comprises 86 institutions from 26 countries



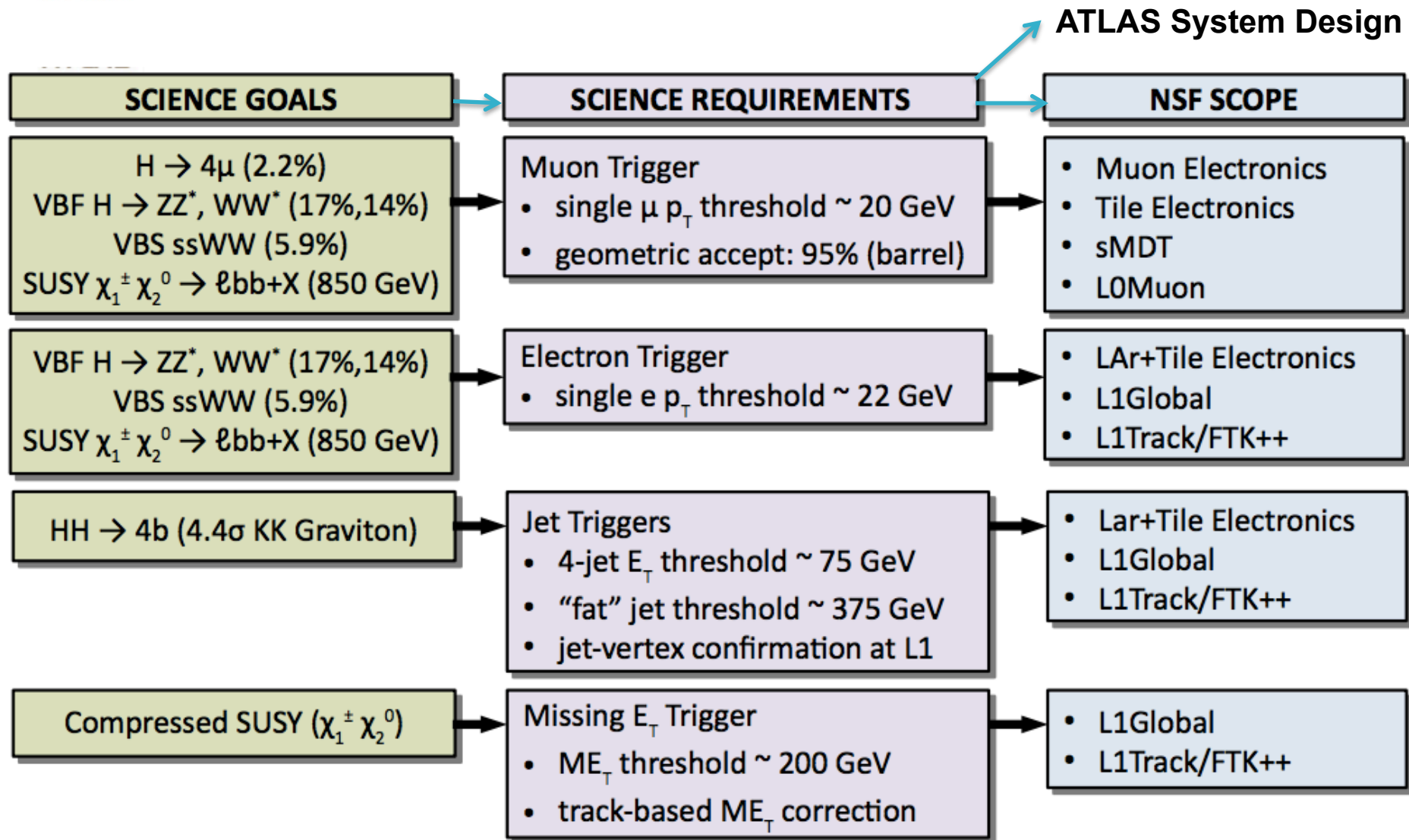
Measurement Goals

- The HL-LHC program is broad
 - Higgs as a tool for discovery
 - Dark matter
 - Exploring the Unknown
 - A representative set of measurements is presented in the PEP document (and in the ATLAS scoping document)

	Channel	Example Quantity	Run 1 Result (25 fb ⁻¹)	Target HL-LHC Sensitivity (3000 fb ⁻¹)
Higgs + Unknown	H → 4μ	Relative uncertainty on production	22%	2.2%
	VBF H → ZZ ^(*) → 4ℓ	Relative uncertainty on production	360%	17% (7.6σ)
	VBF H → WW ^(*) → ℓνℓν	Relative uncertainty on production	36% (3σ)	14% (8.0σ)
Dark Matter + Unknown	VBS ssWW	Relative uncertainty on production	34% (3.6σ)	5.9% (11σ)
Higgs + Unknown	SUSY χ ₁ [±] χ ₂ ⁰ → ℓbb + X	Chargino/neutralino mass	>250 GeV (95% CL)	850 GeV (5σ observation)
	HH → 4b	K-K graviton production	---	4.4σ (at M = 2 TeV)



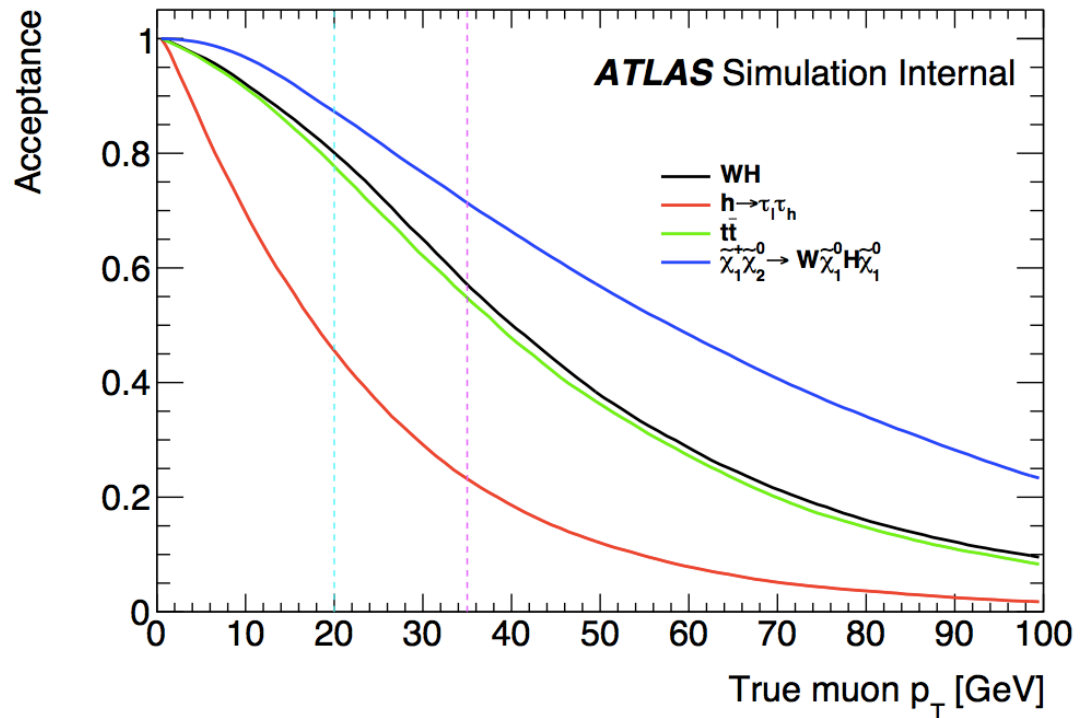
Trigger Flow Down





Threshold Requirements

- **Guideline:** Keep as many events that show evidence of weak scale physics (weak scale = masses of W, Z, and Higgs bosons)
- Single electron or muon triggers at ~ 20 GeV
 - Maintain good acceptance for leptons from W and Z bosons
 - Even more important if physics target favors taus



Upgrade acceptance gain: 25% for $W\chi H\chi$, 40% for $t\bar{t}$ and WH, 75% for $H \rightarrow \tau\tau$

Note: Acceptance gain translates to gain in effective running time



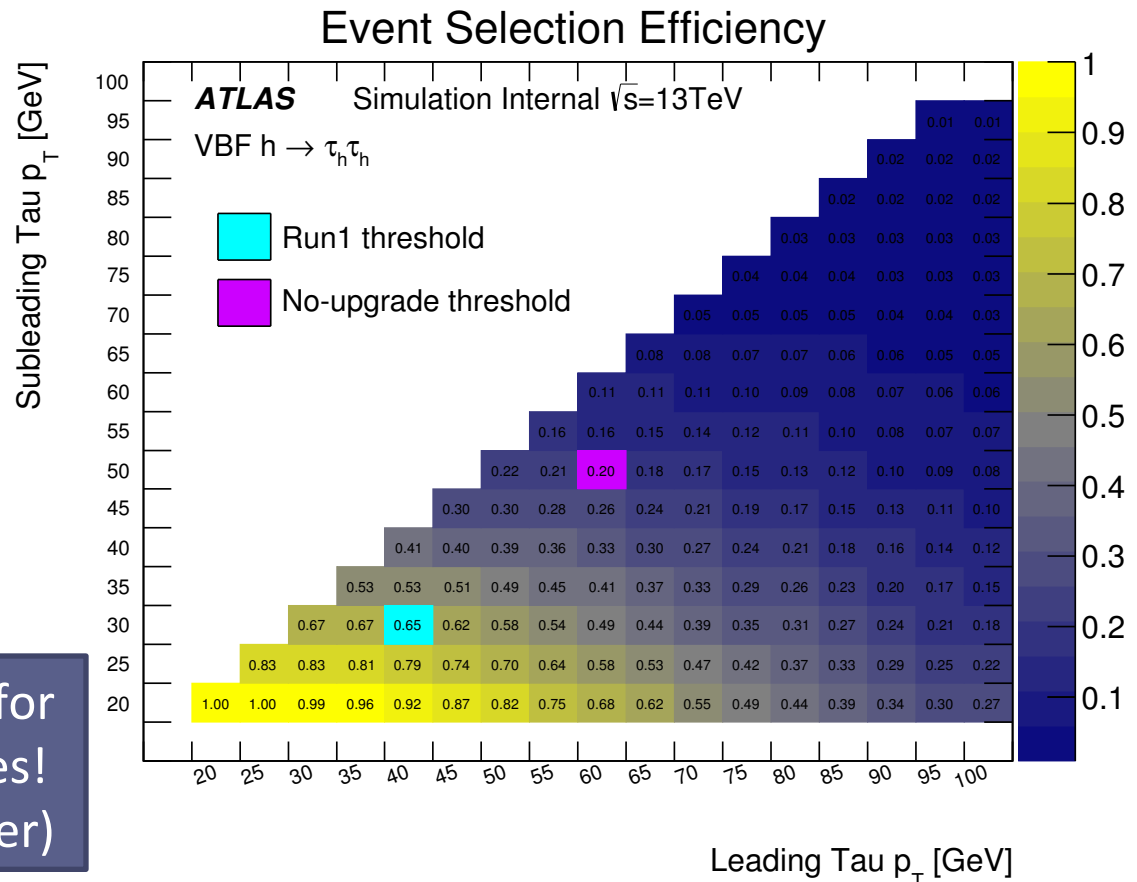
Threshold Requirements

- **Guideline:** Keep as many events that show evidence of weak scale physics (weak scale = masses of W, Z, and Higgs bosons)

- **Di-tau Events**

- Important for many physics channel:
 - $H \rightarrow \tau\tau$
 - Standard model $HH \rightarrow bb\tau\tau$
- SUSY can favor tau in final state

Upgrade acceptance gain for $H \rightarrow \tau\tau$ a factor of 3.3 times!
(similar for dileptons trigger)

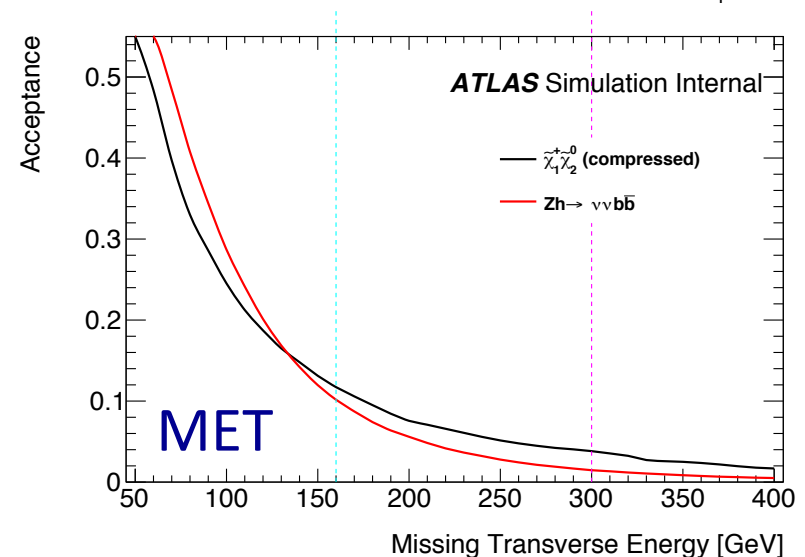
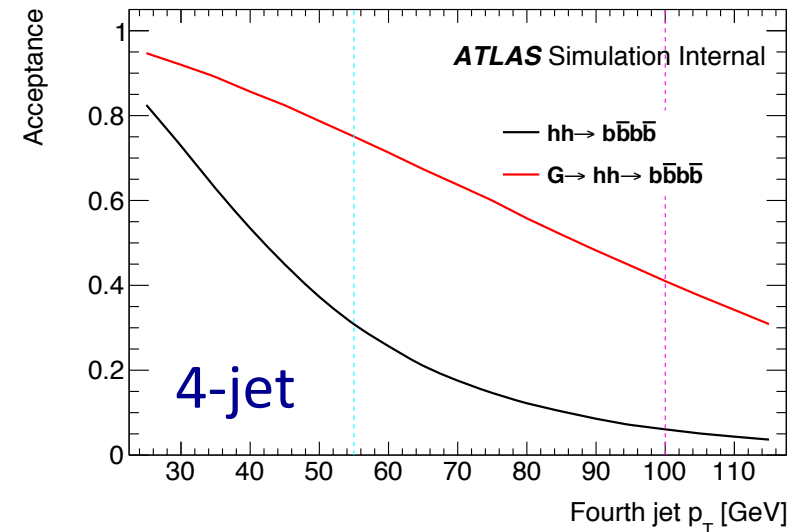




Threshold Requirements

- **Guideline:** Keep as many events that show evidence of weak scale physics (weak scale = masses of W, Z, and Higgs bosons)
- 4-jet events
 - $HH \rightarrow 4b$ (SM or BSM)
 - Diboson searches (= Unknown)
- MET
 - Important for SUSY and Dark Matter
 - $ZH \rightarrow \nu\nu b\bar{b}$

Upgrade acceptance gain
MET: ZH



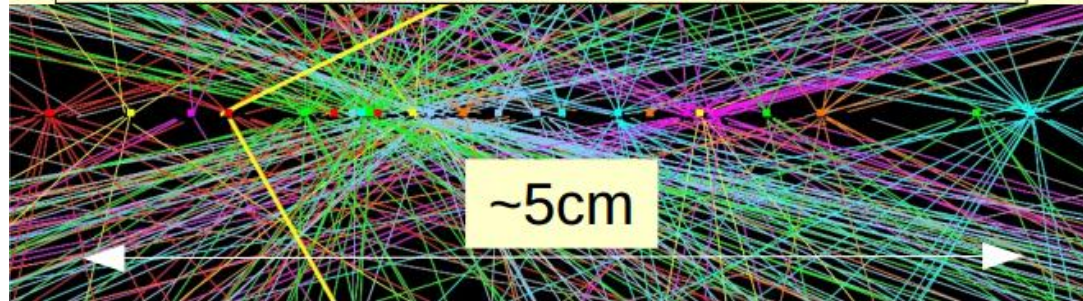


Threshold Requirements

Pile-up and hadronic objects (jets & MET)

- Pile-up is the number of collisions per beam crossing
 - Run 1 pile-up ~ 20
 - HL-LHC pile-up ~ 200

$Z \rightarrow \mu\mu$ event with 25 reconstructed vertices



Tracking is the main tool for differentiating from which vertex something came

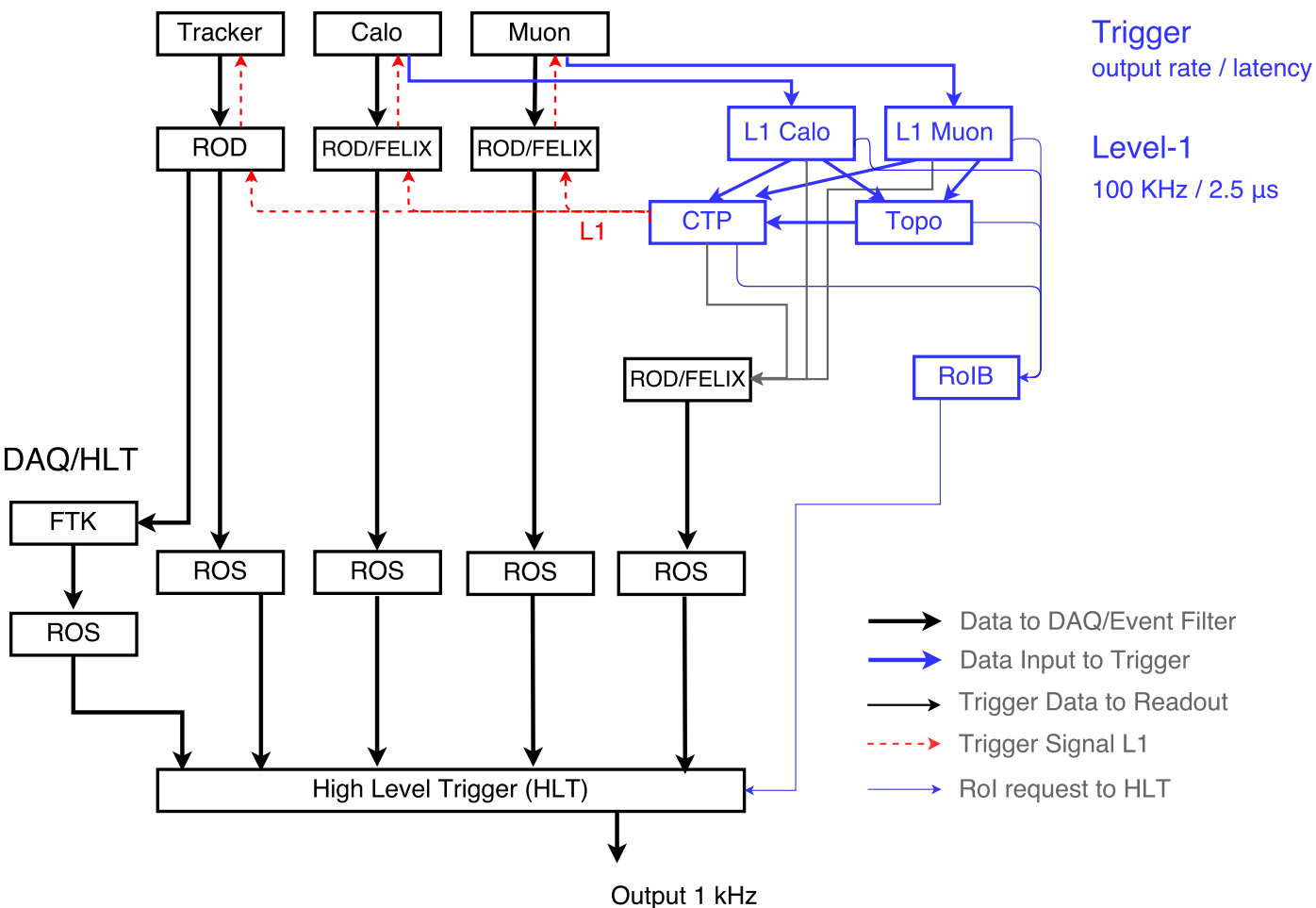
- Tracks are critical in b-jet identification

Tracks are increasingly being used for pile-up suppression in jet & MET

- Run 2 jets used track-based jet energy corrections
 - Most 4-jet events at HL-LHC at the trigger threshold will be from pile-up
- Run 2 MET uses tracking to decide which jets come from the vertex of interest
- Implementation of these for Run 2 is limited by the tracking CPU in the HLT

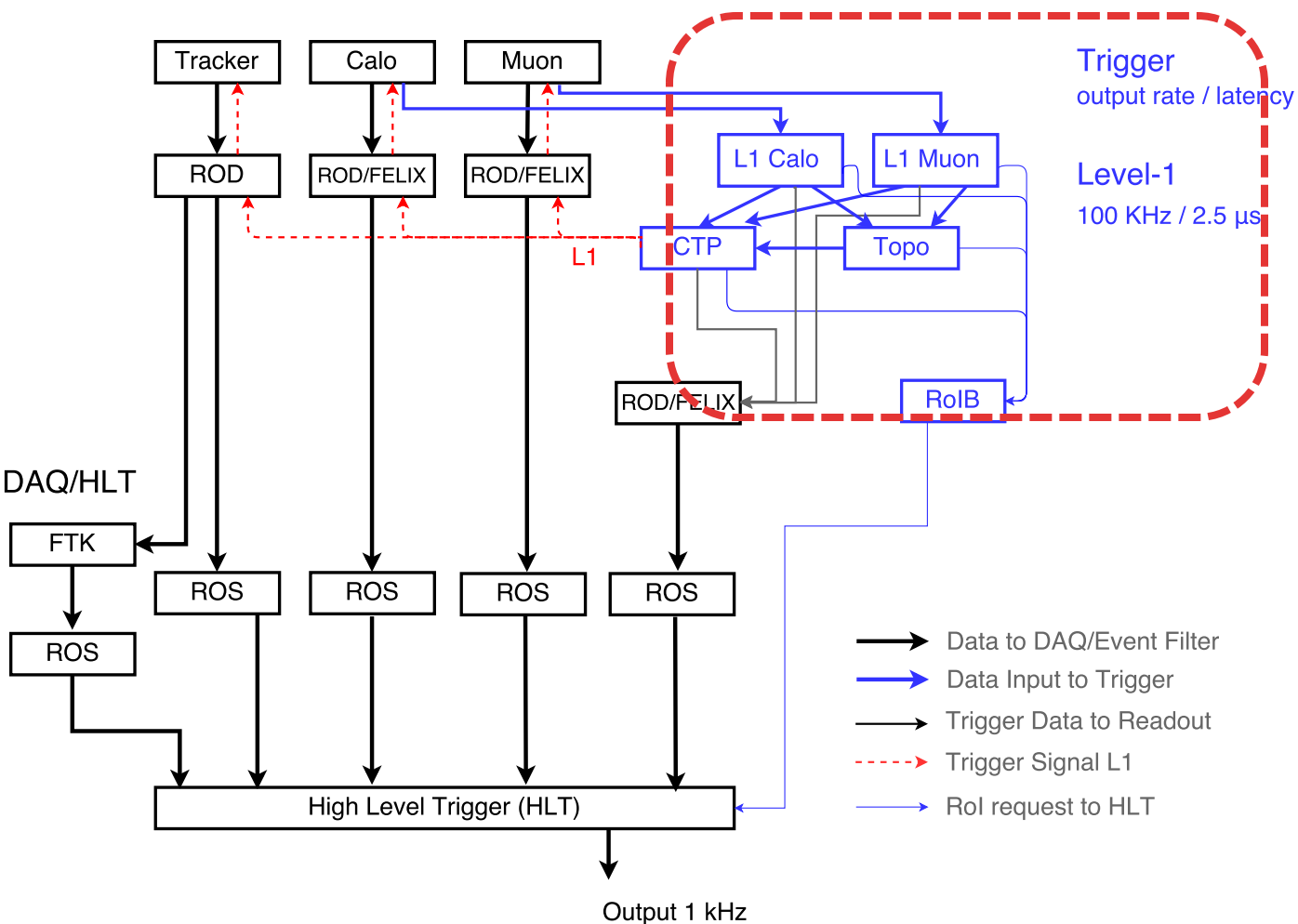
So for online hadronic objects to be compatible with offline with reasonably sharp turn-on curves, tracking is needed as early as possible and as complete as possible

Phase-1 System





Phase-1 System



1 hardware trigger level

- 100 kHz Accept Rate
- 2.5 μ s Latency

Calo

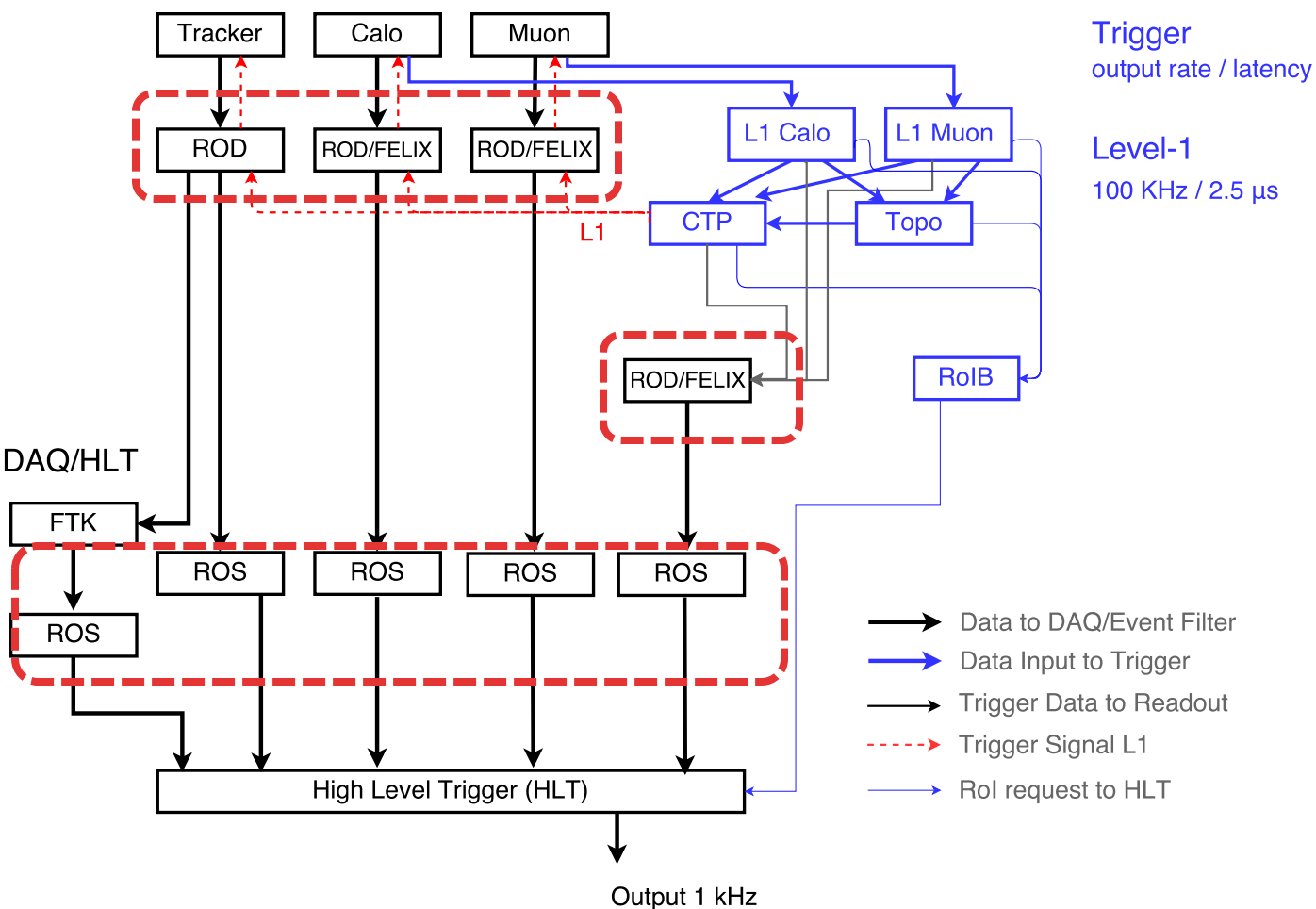
- Course granularity for e, gamma, and jets
- Added course granularity fat jets and global objects (gFEX)

Muon

- Fast detectors only (RPC and TGC)
- “New small wheel” (NSW) improves fake rejection in endcap



Phase-1 System



Data then readout via DAQ system

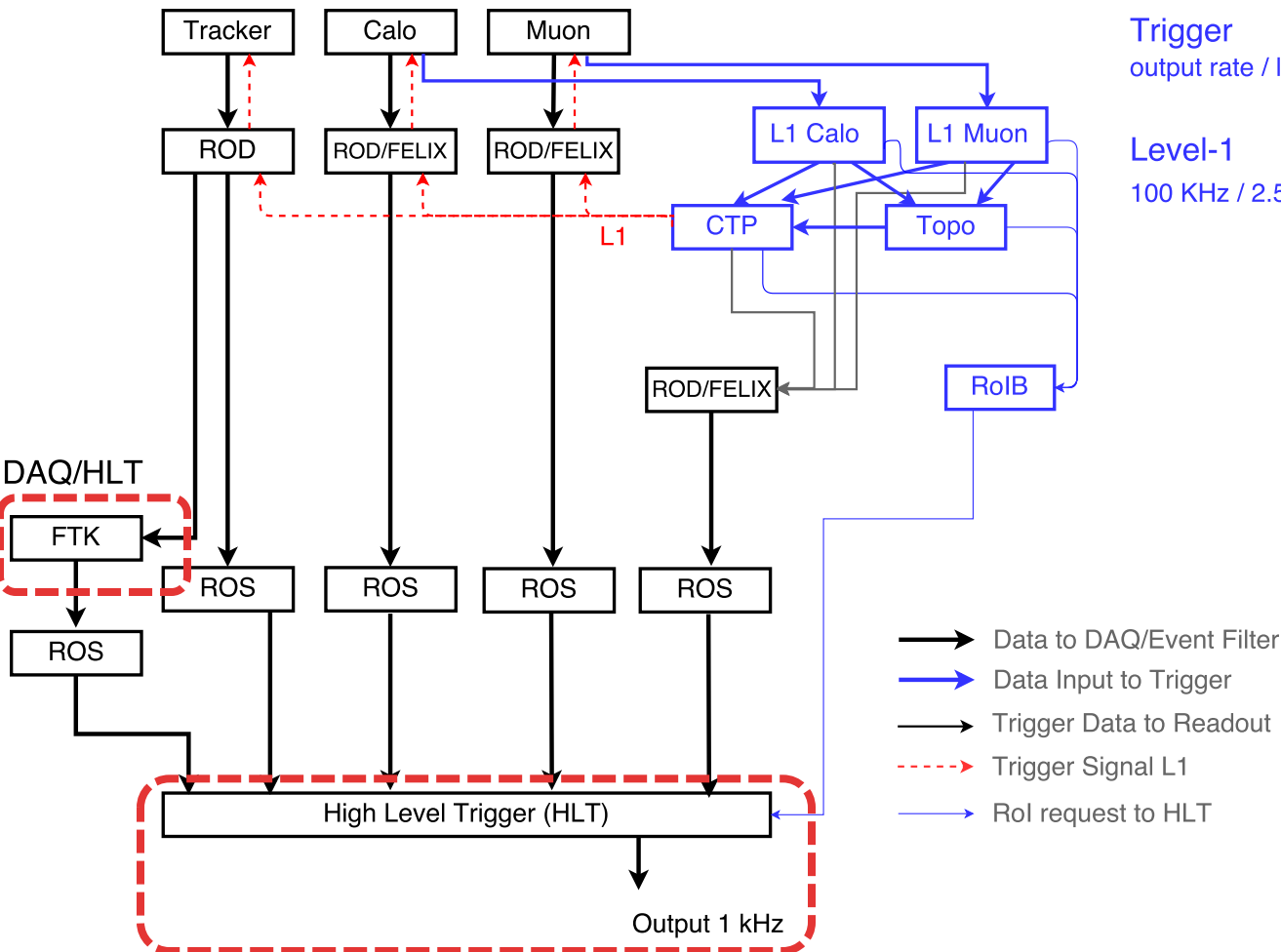
- Data aggregated and buffered

Trigger
output rate / latency

Level-1
100 KHz / 2.5 μ s



Phase-1 System



Trigger
output rate / latency

Level-1
100 KHz / 2.5 μ s

“High-Level Trigger”

- PC-based farm
- Adds tracking using Hardware preprocessor for track reconstruction (FTK)
- Adds full granularity calorimeter information
- Adds high precision muon chamber (MDT) information
- Output rate 1 kHz



Phase-1 System Limitations

General Physics Goal: Threshold goals similar to Run 1 thresholds

- These thresholds are proven to support a broad physics program

Phase-1 hardware at HL-LHC luminosity for
Target Thresholds (~Run1)

Many triggers in excess to
100 KHz (= the Phase-1 limit)

Item	Run 1 Offline p_T Threshold [GeV]	Phase-I Level-1 system performance at $L = 7.5 \times 10^{34} \text{cm}^{-2}\text{s}^{-1}$	
		Offline Threshold for Phase-II Goal [GeV]	Level-1 Rate [kHz]
isolated Single e	25	22	200
single μ	25	20	40
di- γ	25	25	8
di- e	17	15	90
di- μ	12	11	10
$e - \mu$	17,6	17,12	8
single τ	100	150	20
di- τ	40,30	40,30	200
single jet	200	180	60
four-jet	55	75	50
E_T^{miss}	120	200	50
jet + E_T^{miss}	150,120	140,125	60

Including key single
electron trigger

Would need to raise
electron threshold to
~35-40 GeV

} Hadronic triggers
allowed to degrade
somewhat

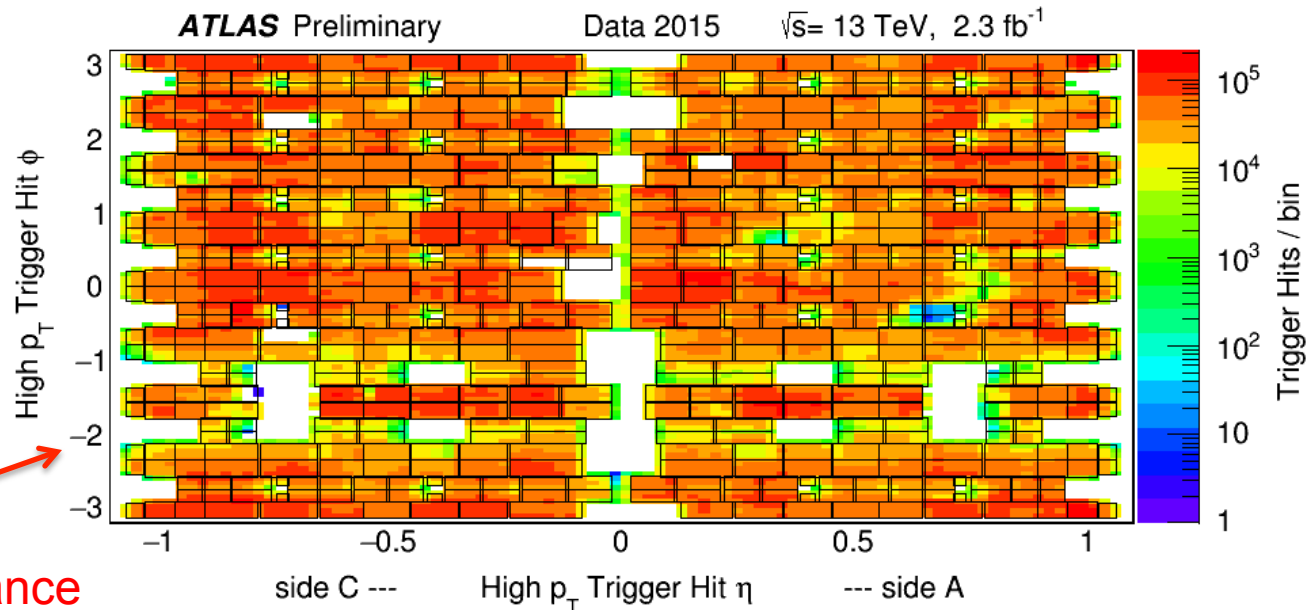
Offline thresholds that can be used
with the associated trigger



Phase-1 System Limitations

Another Key Issue:
Low muon trigger efficiency of Phase-1 system

RPC chamber acceptance has lots of holes



Because RPC chamber (barrel) need to be run at reduced voltage to avoid aging, barrel efficiency would be further reduced to 65%.

- Bad for single muon trigger, *really* bad for dimuon triggers

Addressed by a combination of new RPCs and using high precision MDT chambers in trigger which improves the 65% to 95%



System Design

Two hardware trigger levels

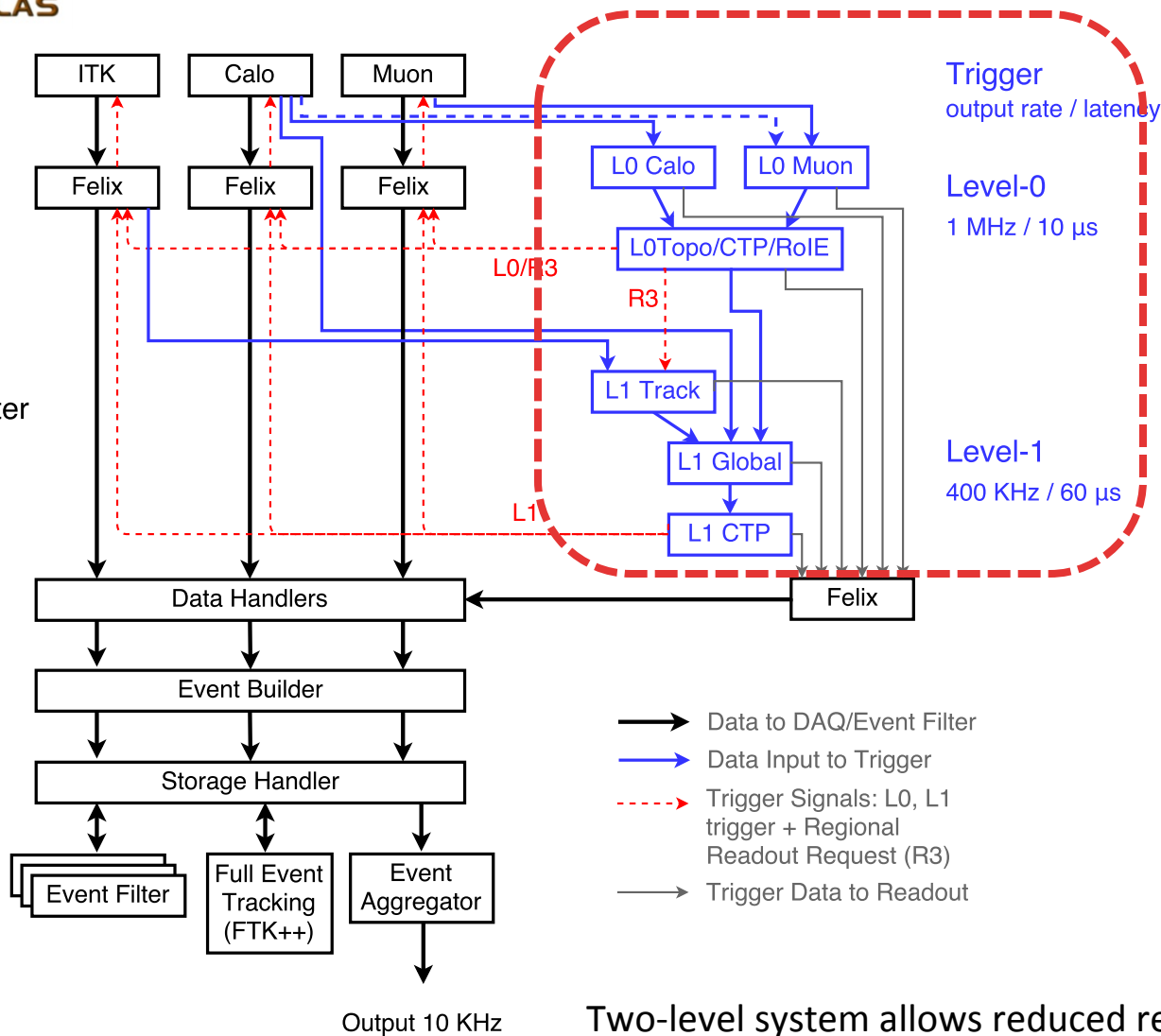
Level 0 (L0)

- 1 MHz L0 Accept Rate
- 6/10 μ s Latency
- 6 μ s = Trigger Target
- 10 μ s = Detector Req.
- Difference is a contingency

Level 1 (L1)

- 400 kHz L1 Accept Rate
- 30/60 μ s Latency

DAQ /
Event Filter



- Data to DAQ/Event Filter
- Data Input to Trigger
- - - - - Trigger Signals: L0, L1 trigger + Regional Readout Request (R3)
- Trigger Data to Readout

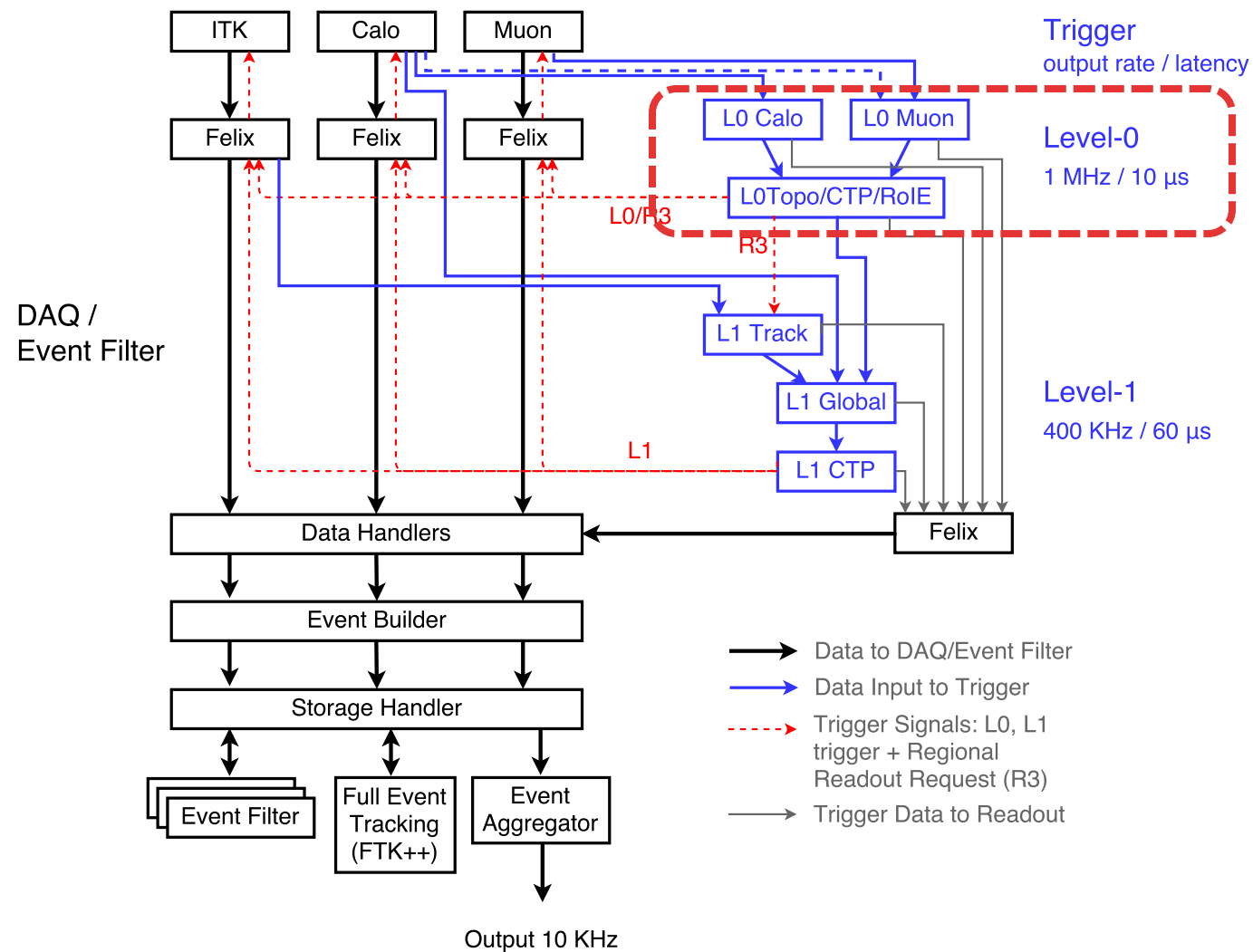
Two-level system allows reduced readout bandwidth requirements on detectors (compatible with legacy electronics)



System Design

Level 0 (L0)

- Input 40 MHz
- Output 1 MHz
- Same hardware as Phase-1 L1 trigger
- Extended to have High Precision Muon Chambers (MDT) → improves efficiency
- Higher accept rate (100 kHz → 1 MHz) means higher physics acceptance



System Design

Level 1 (L1)

- Input 1 MHz
- Output 400 kHz
- Tracking in regions of interest (L1Track)
 - 10% of data at 1 MHz
- Full granularity calorimetry combined with tracking in regions of interest to improves rejection before HLT (L1Global)

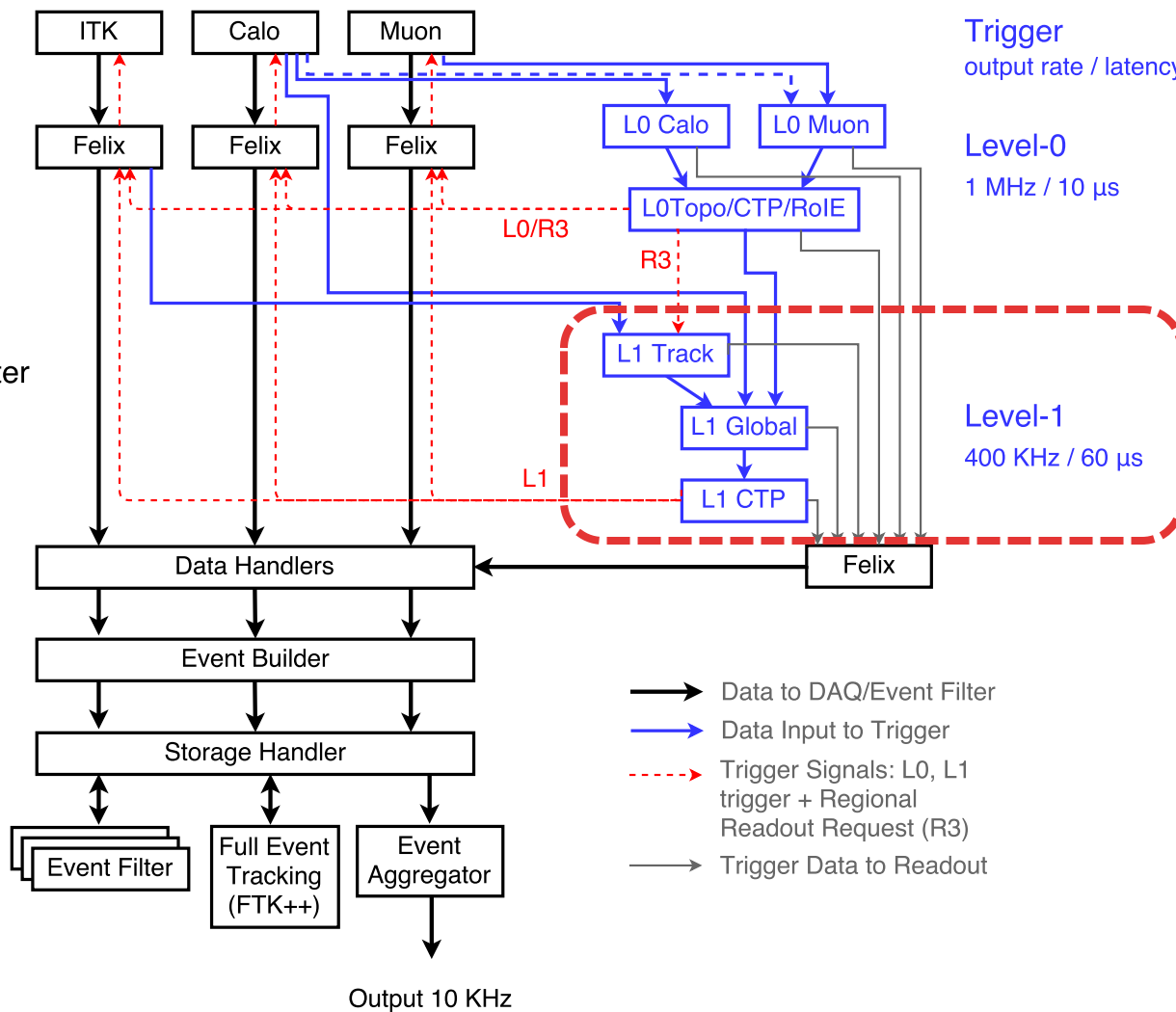
Trigger
output rate / latency

Level-0
1 MHz / 10 μ s

Level-1
400 KHz / 60 μ s

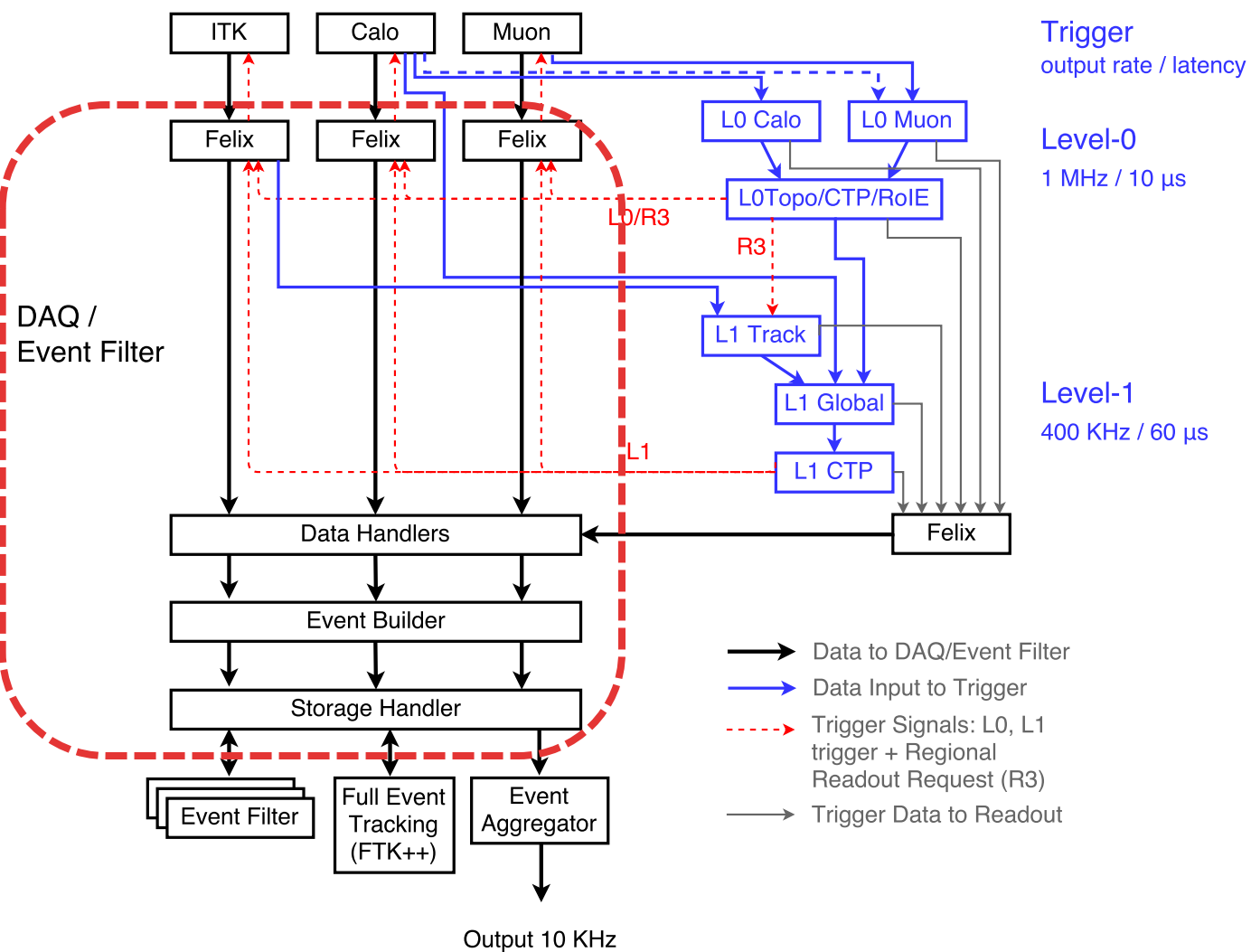
- Data to DAQ/Event Filter
- Data Input to Trigger
- - - - - Trigger Signals: L0, L1 trigger + Regional Readout Request (R3)
- Trigger Data to Readout

DAQ /
Event Filter



Output 10 KHz

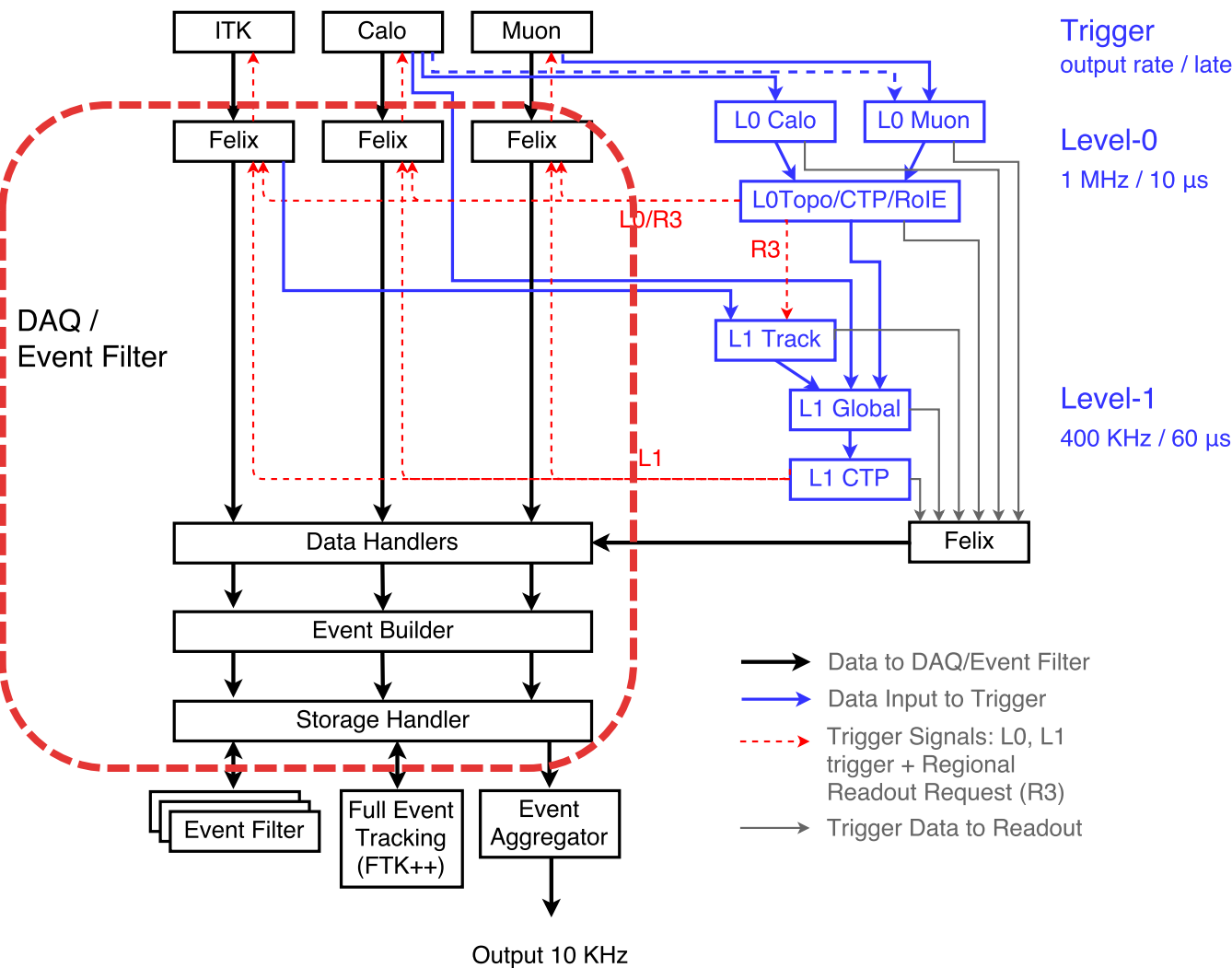
System Design



DAQ System

- Data aggregated and buffered

System Design



Event Filter System

- Input 400 kHz
- Output 10 kHz
- PC-based farm
- With hardware-based tracking co-processor (FTK++) which provides 100 kHz full-detector tracking
- Offline-like algorithms assure no loss in effective threshold due to incompatibility

Trigger
output rate / latency

Level-0
1 MHz / 10 μ s

Level-1
400 KHz / 60 μ s

- Data to DAQ/Event Filter
- Data Input to Trigger
- - - - - Trigger Signals: L0, L1
trigger + Regional
Readout Request (R3)
- Trigger Data to Readout



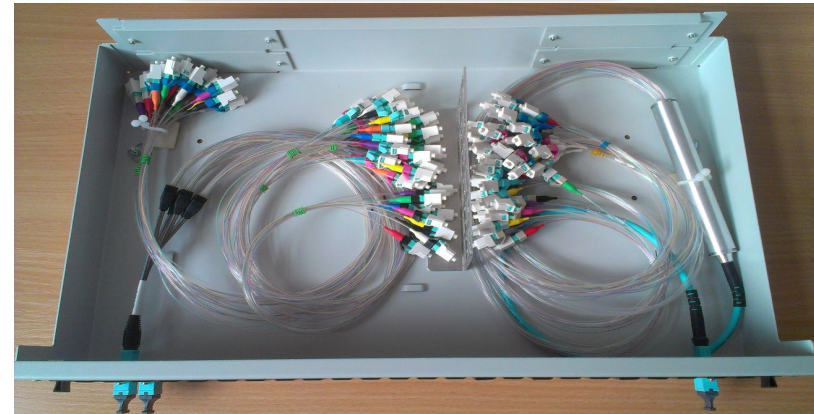
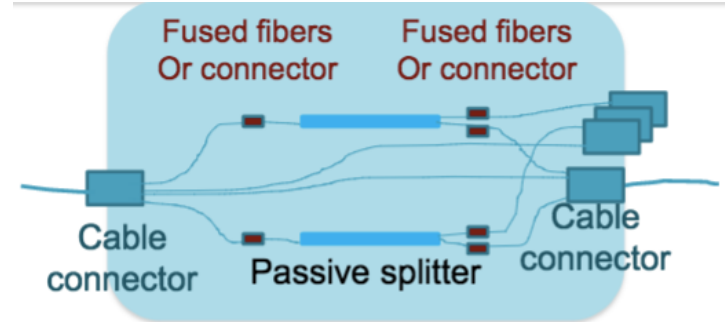
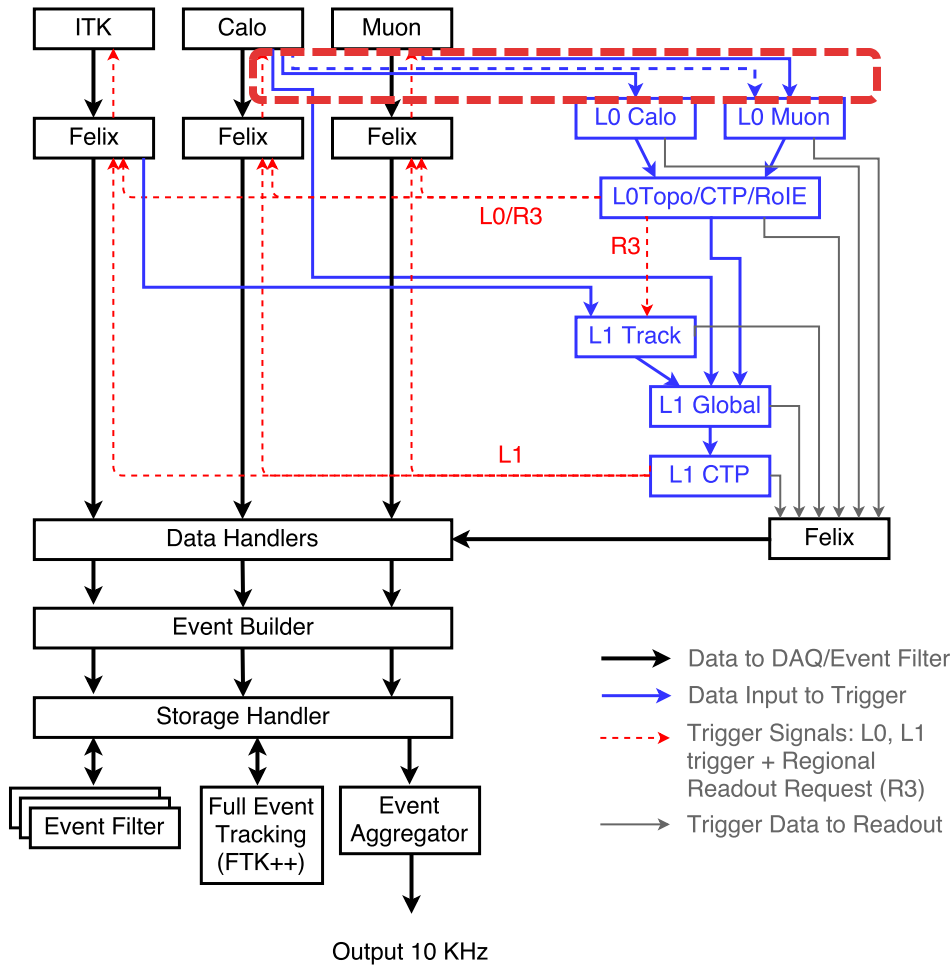
US Involvement

- 17 US institutions in ATLAS Trigger/DAQ group
- US institutions play a key role in the overall management of the ATLAS Trigger/DAQ group
 - David Strom (Oregon) is one of two Trigger/DAQ managers
 - Chris Bee (Stonybrook) is Institute Board Chair
- The US has played a strong role in the trigger hardware for the Phase-1 upgrade
- US institutes involved in HL-LHC construction plan
 - U of California (Irvine)
 - University of Chicago
 - U of Illinois (Urbana-Champaign)
 - Indiana University
 - University of Oregon
 - University of Pennsylvania
 - University of Pittsburgh
 - Louisiana Tech
 - Michigan State University
 - Northern Illinois University
 - Stanford

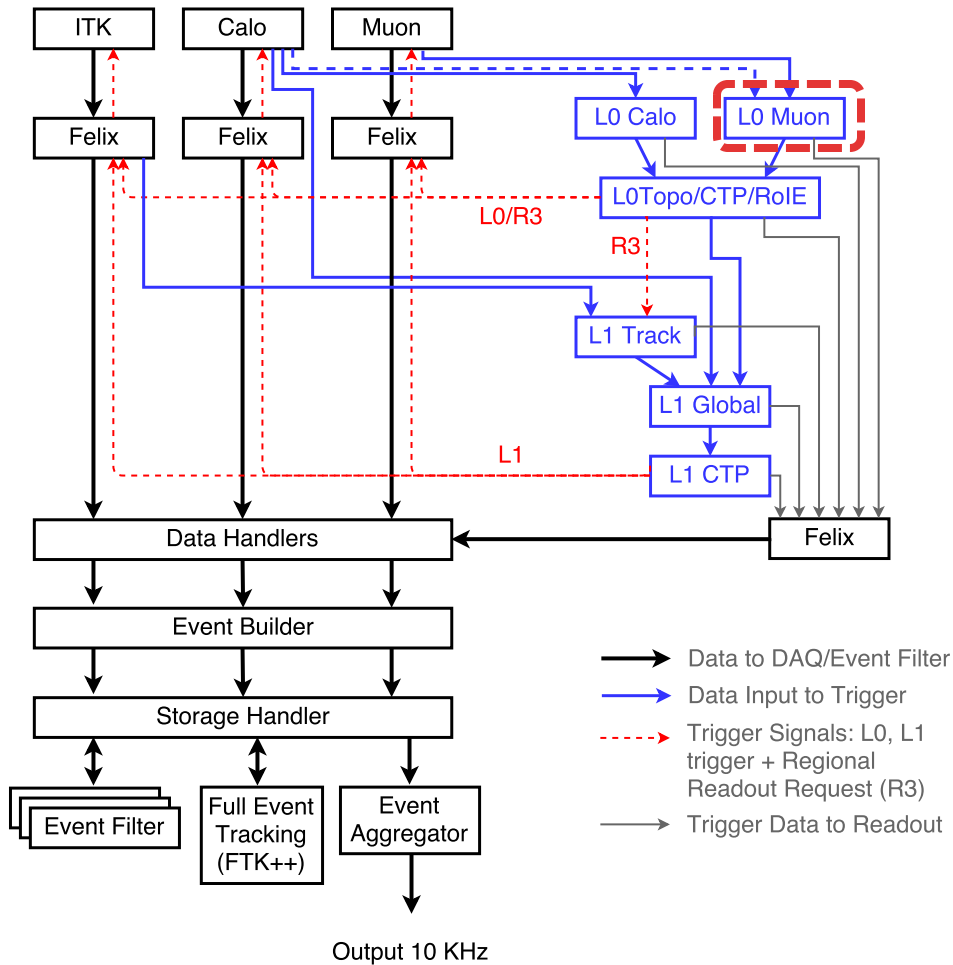
Proposed NSF Scope

6.8.y.1 L0 Calo

- Rebuild fiber optic input router because of changes to tile inputs
 - Passive optical router maps and splits fiber signals to prep pattern recognition
- MSU is building Phase-1 system this capitalizes on their unique expertise
- Institutes:** Michigan State (MSU)

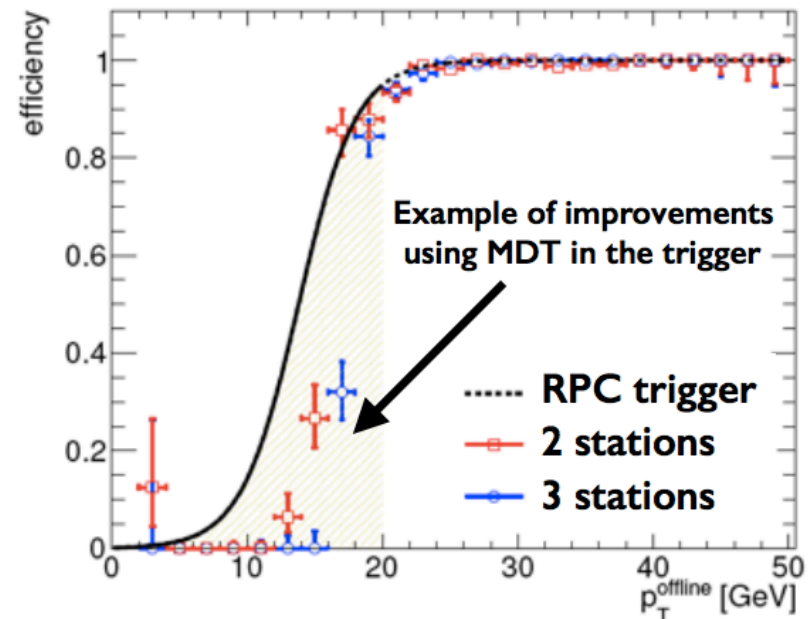


Proposed NSF Scope



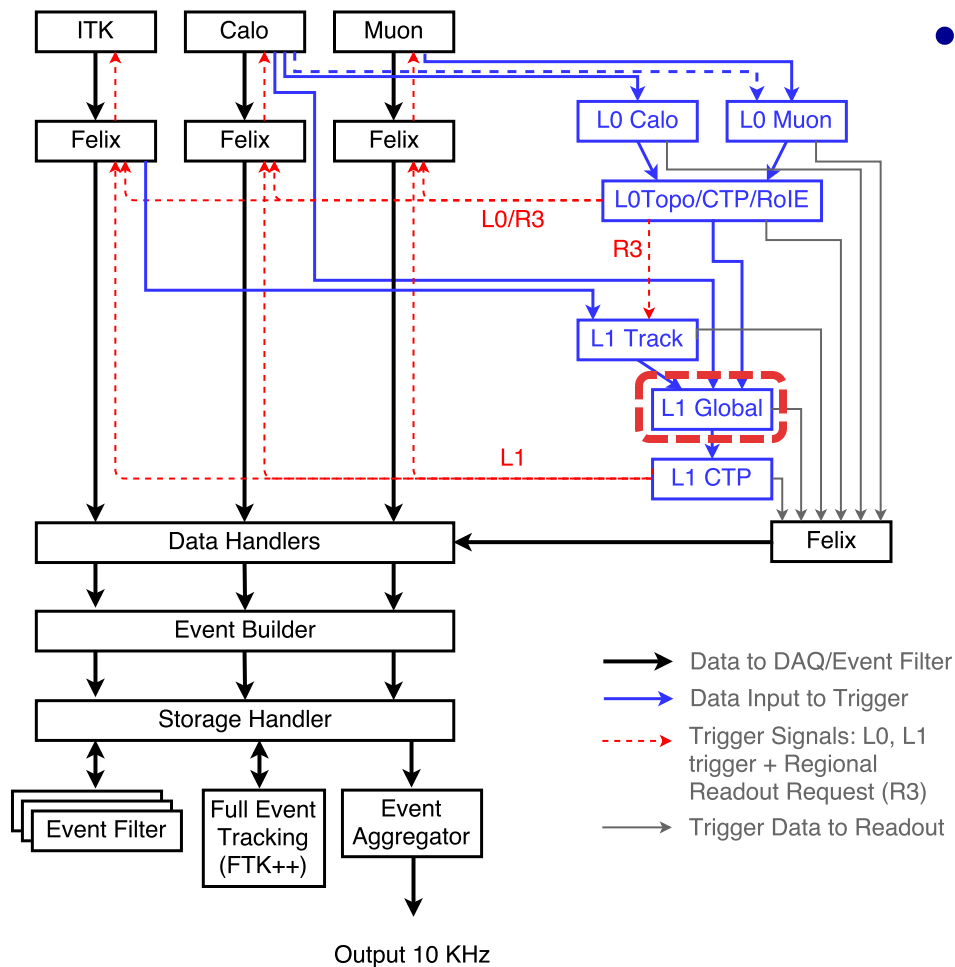
6.8.y.2 L0 Muon

- Processing mezzanine boards for MDT (high-precision chambers) trigger with firmware (32 boards)
- Sharpens muon turn-on curve, reduces rates, improves efficiency
 - Key for high efficiency, low rate single muon trigger
- Institutes: UC Irvine





Proposed NSF Scope

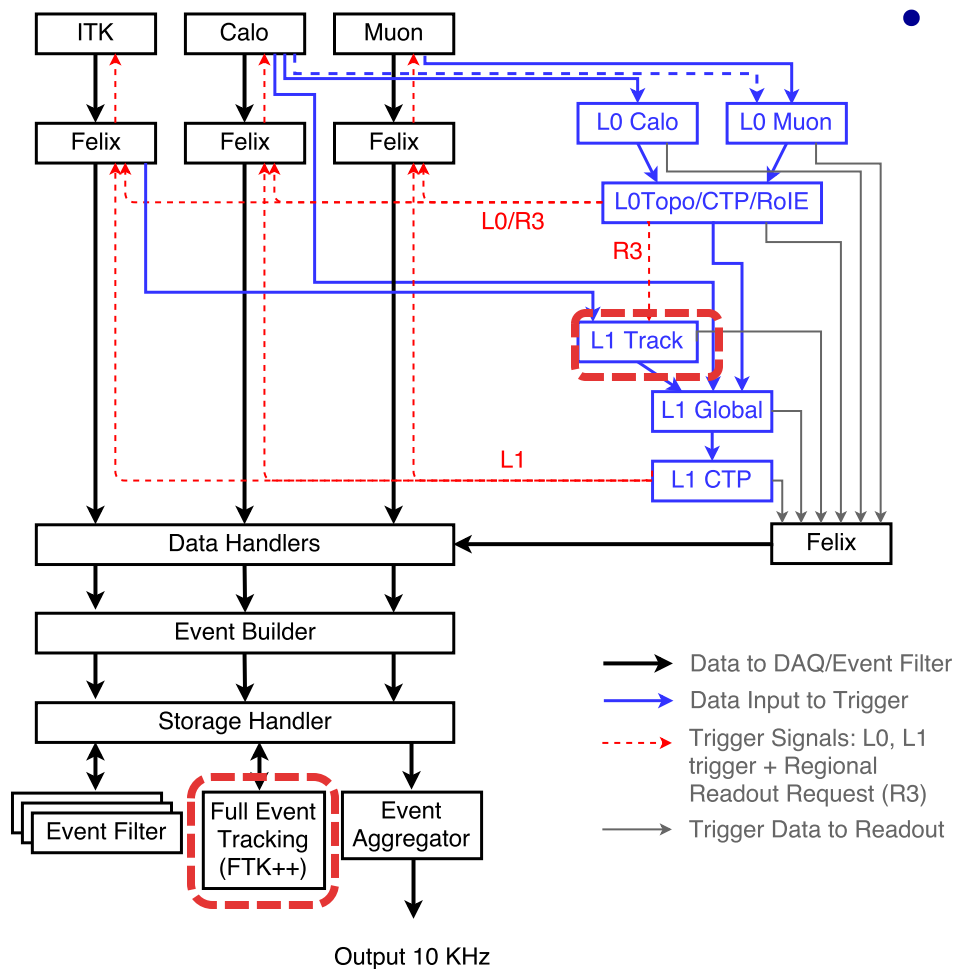


6.8.y.3 L1 Global Processing

- L1 Global algorithms are where the rate reduction from 1 MHz to 400 KHz happens
- 4 firmware algorithms focus on hadronic triggering:
 - Offline-like energy clustering
 - Offline-like Jet construction
 - Global quantities (MET, HT)
 - Track-based pile-up rejection
- This builds on US experience with Phase-1 “gFEX” system which does global hadronic triggering in what will be L0
- **Institutes:** U Chicago, U Indiana, Louisiana Tech, Michigan State, U Oregon, U Pittsburgh



Proposed NSF Scope



- 6.8.y.4 L1Track/FTK++ Processing
 - L1Track provides regional tracking at 1 MHz at low-latency as input to L1 Global
 - Many many uses... key for electron, tau, and multiobject hadronic triggers
 - FTK++ provides full detector tracking to be used in the Event Filter (PC farm)
 - This is expected to be critical for maintaining sharp turn-on curves for offline definitions of jets and MET that involve tracking and also for maintaining low p_T thresholds for multi b-jet triggers
 - 690 mainboards (data preparation) and 1104 track-fitting mezzanines with firmware
 - Capitalizes on US experience on the Phase-1 FTK system
 - Institutes:** U Chicago, U Illinois Urbana-Champaign, U Indiana, Northern Illinois University, U Penn, Stanford,



The ATLAS Trigger Project

ATLAS WBS	ATLAS Item (Scoping Doc)	US WBS	Deliverable	NSF Fraction	
				Design	Production
1	TDAQ System	6.8	Trigger	22% of Trigger Items	
1.1	L0 Central				
1.1.1	LOCTP				
1.1.2	MuCTPi				
1.1.3	RoI Distributor				
1.2	L0 Central				
1.2.1	FEX				
1.2.2	Topo Proc.				
1.2.3	Optical Plant	6.8.x.1	L0 Calo	100%	100%
1.2.4	L0Calo-to-L1Calo				
1.3/1.4	L0 Muon Barrel/Endcap				
1.3.1/1.4.1	RPC/TGC Sector Logic				
1.3.2/1.4.2	MDT Trigger Mainboard				
	Mezzanine	6.8.x.2	L0 Muon	100%	100%
1.5	L1 Central				
1.5.1	L1CTP				
1.5.2	TTC				

Continued next slide...



The ATLAS Trigger Project

ATLAS WBS	ATLAS Item (Scoping Doc)	US WBS	Deliverable	NSF Fraction Design	NSF Fraction Production
1.6	L1 Global				
1.6.1	Aggregator				
1.6.2	Event Processor				
	Hardware				
	Algorithms	6.8.x.3	L1 Global Processing	50%	50%
= 100% of hadronic objects					
1.7/1.8	L1 Track/FTK++				
1.7.1/1.8.1	Processing				
	Mainboard	6.8.x.4	L1Track/FTK++ Processing	100%	50%
	RTM				
	AM Chip				
	Mezzanine				
1.7.2/1.8.2	Second Stage				
	Mainboard	6.8.x.4	L1Track/FTK++ Processing	100%	50%
	RTM				
	Mezzanine	6.8.x.4	L1Track/FTK++ Processing	100%	100%
1.9	DAQ				
1.9.1	Detector Readout				
1.9.2	Dataflow				
1.9.3	Event Filter				

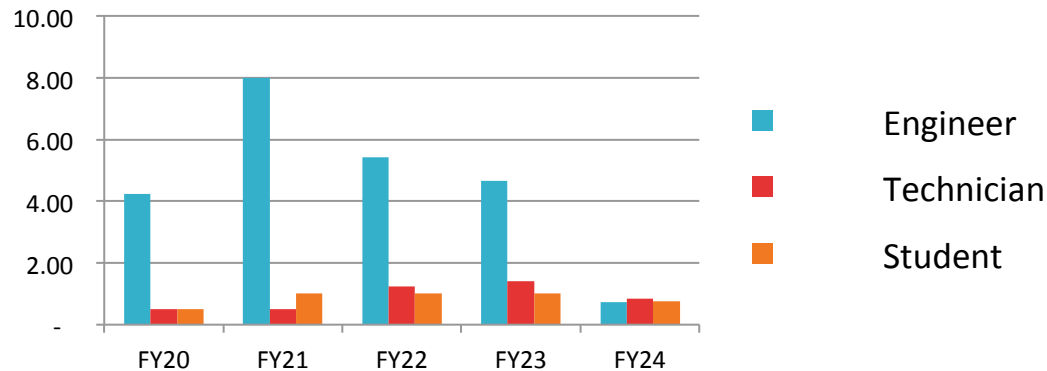


Budget

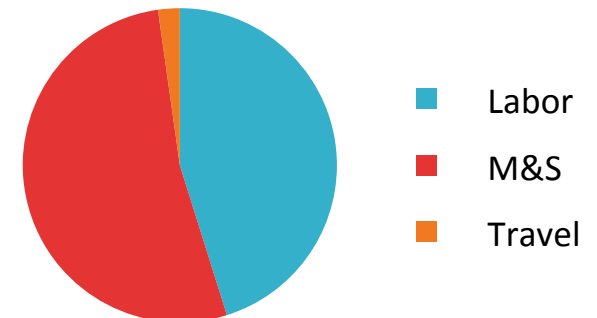
6.8 Trigger NSF Total Cost (AYk\$)

Item/Phase	FY20	FY21	FY22	FY23	FY24	Total
6.8.y.1 L0 Calo	0	43	126	19	0	187
6.8.y.2 L0 Muon	265	455	466	778	291	2,256
6.8.y.3 L1 Global Processing	337	611	569	586	0	2,103
6.8.y.4 L1 Track/FTK++Processing	594	835	1,054	5,598	51	8,132
NSF Grand Total	1,197	1,943	2,215	6,980	343	12,678

WBS 6.8 Trigger NSF Labor Types



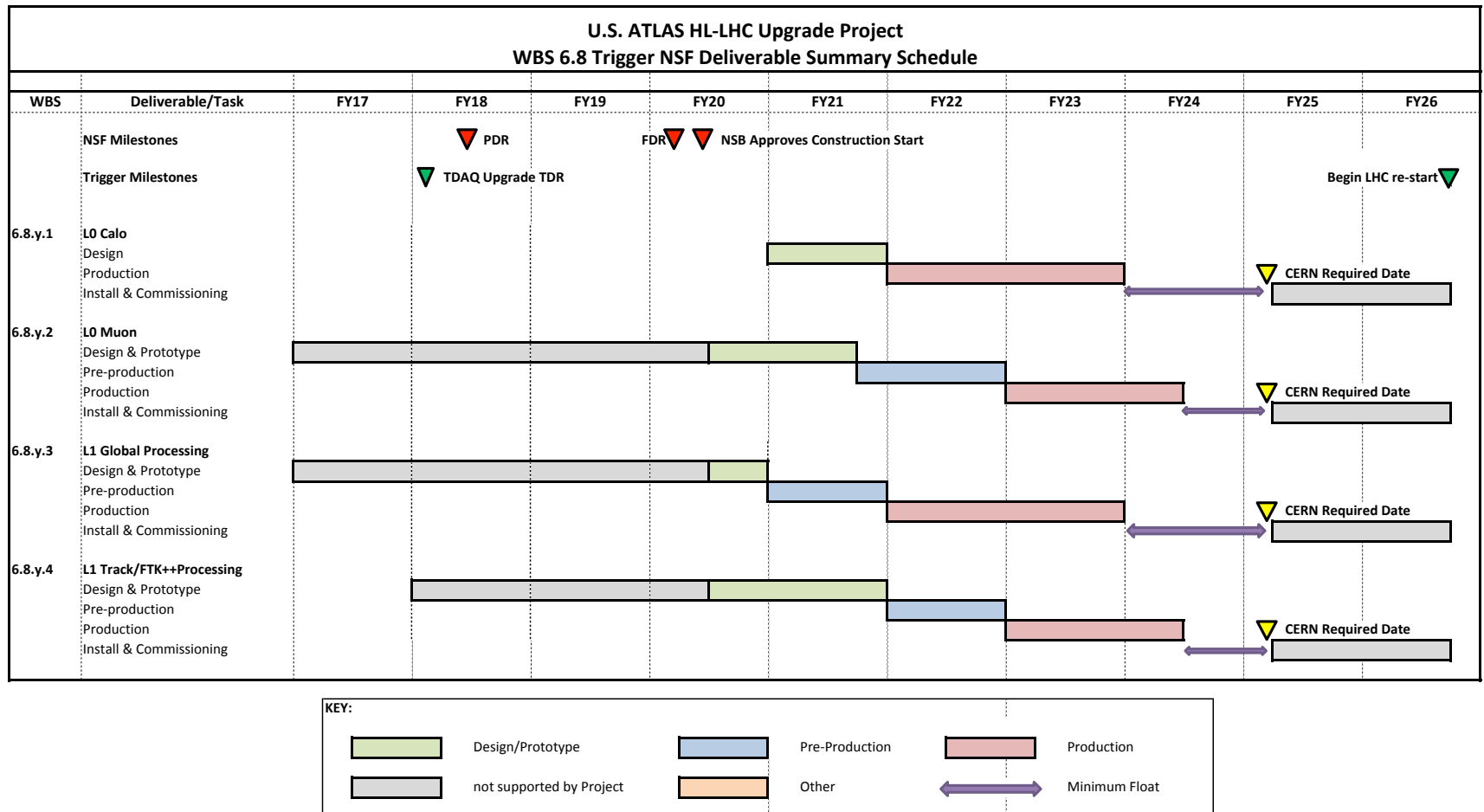
WBS 6.8 Trigger L2 NSF Resource Breakdown





Schedule

- Schedule based on Analogous Phase-1 experience



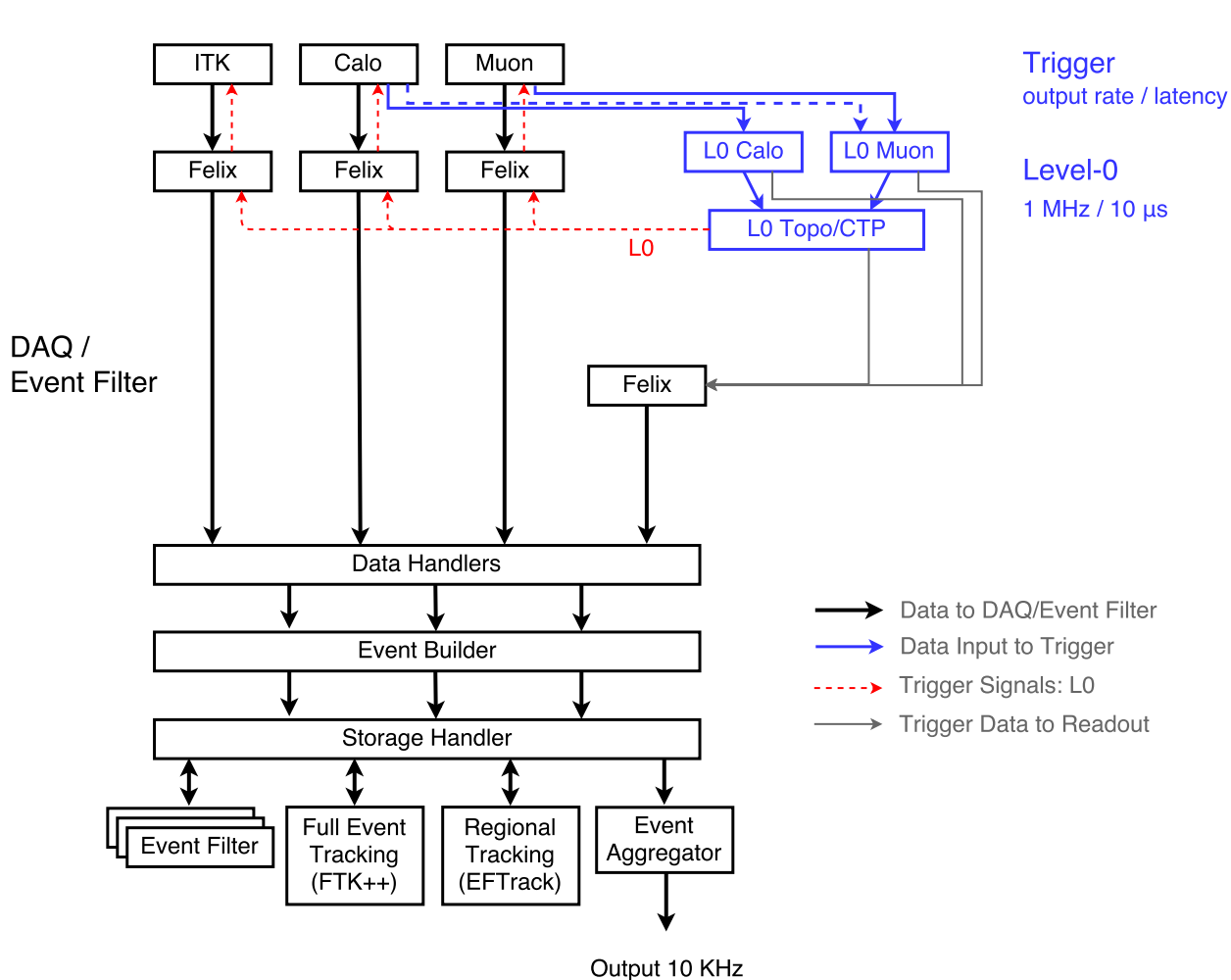


Milestones

- TDAQ IDR will be reviewed early 2016
- IDR will contain two design options
 - L0/L1 system as described in this talk which is described in the Lol and the scoping document
 - A single-level hardware system where the L1 decisions is transferred to the Event Filter (PC farm)
 - The decision date for this is expected to be summer 2016
- TDAQ TDR is scheduled for end-2017



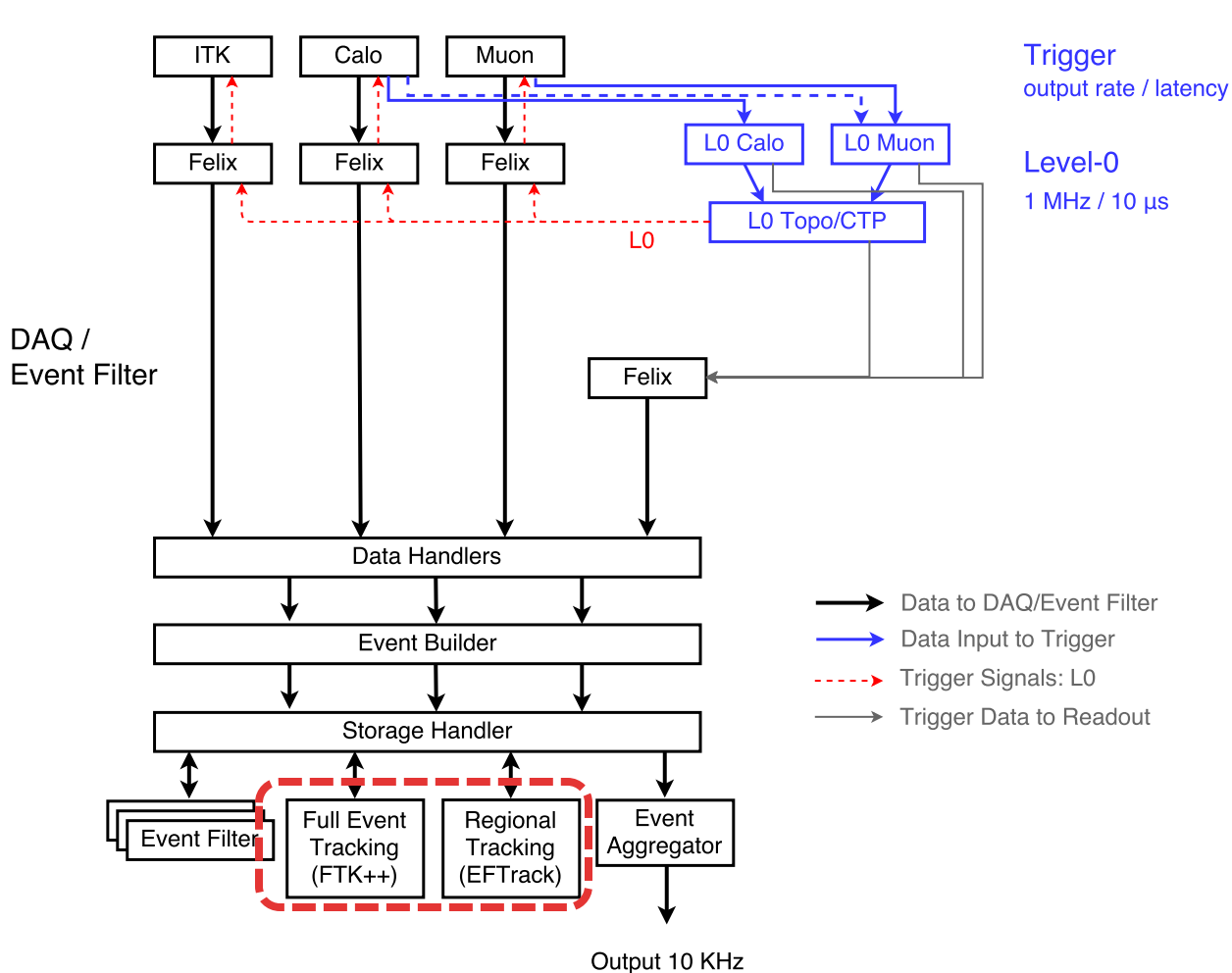
Single-Level vs L0/L1 split



- There is discussion in ATLAS to consider the possibility of removing the L0/L1 split
- In this scenario the HLT does all the work that the L1 previously did



Single-Level vs L0/L1 split

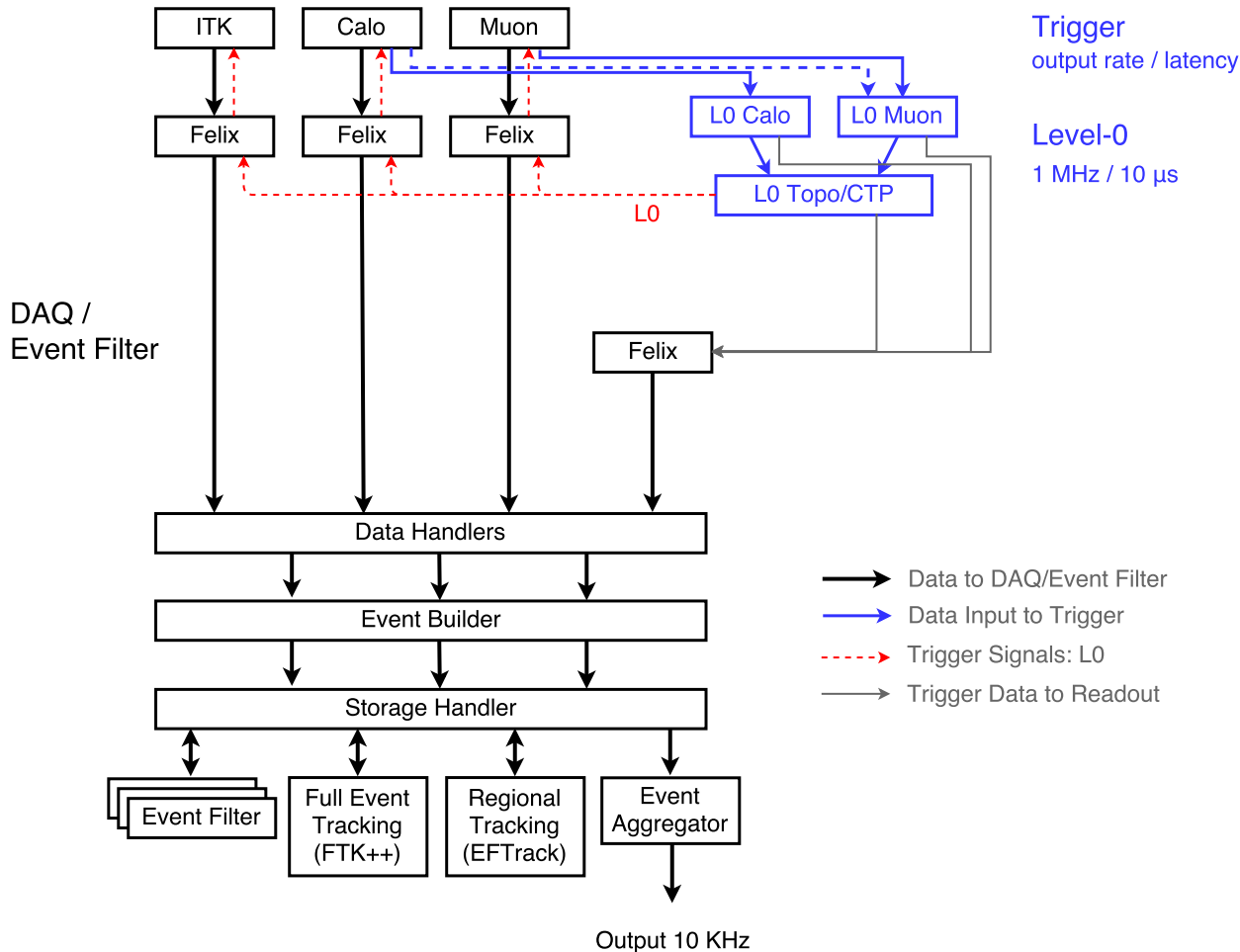


- There is still a need for high-rate tracking in hardware

- Relatively small impact on plan
- L1Track/FTK++ will be reconfigured, but hardware is likely to still exist



Single-Level vs L0/L1 split



- The L1Global functionality to process high granularity calorimeter information at a high rate is still needed, but it could take a very different form
- Their many options being considered, none of which have been studied in detail

- Preprocessing in LAr and Tile preprocessors?
- GPU/CPU(?) processing in augmented EF farm?
- Move L1Global to L0Global?



Risks

- General sources of risk
 - Changes or delays in system definition
 - Changes or delays in interfaces with other sub-systems
 - Performance of available FPGAs or other processors different than expected
- Mitigation
 - In general, mitigation is system specific
 - In some cases, development can continue even when system definitions are not complete
 - Performance issues can be handled by reducing target efficiencies if necessary



Scope Contingency

Scope Contingency

- Early Decision ~ FY20
 - Remove one L1 Global algorithm -\$380k
 - ATLAS management finds non-US replacement or some selection is not refined in L1 Global (end up raising a threshold)
- Late Decision ~ FY22
 - 30% instead of 50% L1Track/FTK++ mainboards \$-1140k
 - ATLAS management finds non-US replacement or the efficiency/coverage will be reduced

Scope Opportunity

- Early Decision ~ FY20
 - add one L1 Global algorithm +\$380k



Research & Development

- 6.8.y.1 L0 Calo
 - Fiber plant is similar enough to Phase-1 that no early R&D is needed
- 6.8.y.2 L0 Muon to start in FY17
 - Preliminary algorithm with timing in FPGA, latency estimate for TDR (end-2017)
 - Then continued development of algorithm and infrastructure in development board
- 6.8.y.3 L1 Global processing
 - has begun to better understand how to implement iterative cluster finding in FPGAs, will give input on processor selection
- 6.8.y.4 L1Track/FTK++ Processing
 - Starting in FY18, mainboard studies include barebones test board for full mesh ATCA interaction
 - Starting in FY18, mezzanine prototype board to test FPGA to memory speeds (give input to FPGA/memory selection)



Closing Remarks

- US Deliverables
 - 6.8.y.1 L0 Calo fiber optic plant for new tile output
 - 6.8.y.2 L0 Muon MDT segment finding and fitting mezzanine
 - 6.8.y.3 L1 Global Processing algorithms for hadronic objects
 - 6.8.y.4 L1Track/FTK++ mainboard and second stage fitting mezzanines
- This package will have a high impact on the ability of ATLAS to maintain low threshold single lepton and hadronic triggers
 - Which is key to the science goals and maintain a broad physics program
- Budget and Planning are based on Phase-1 experience



Backup

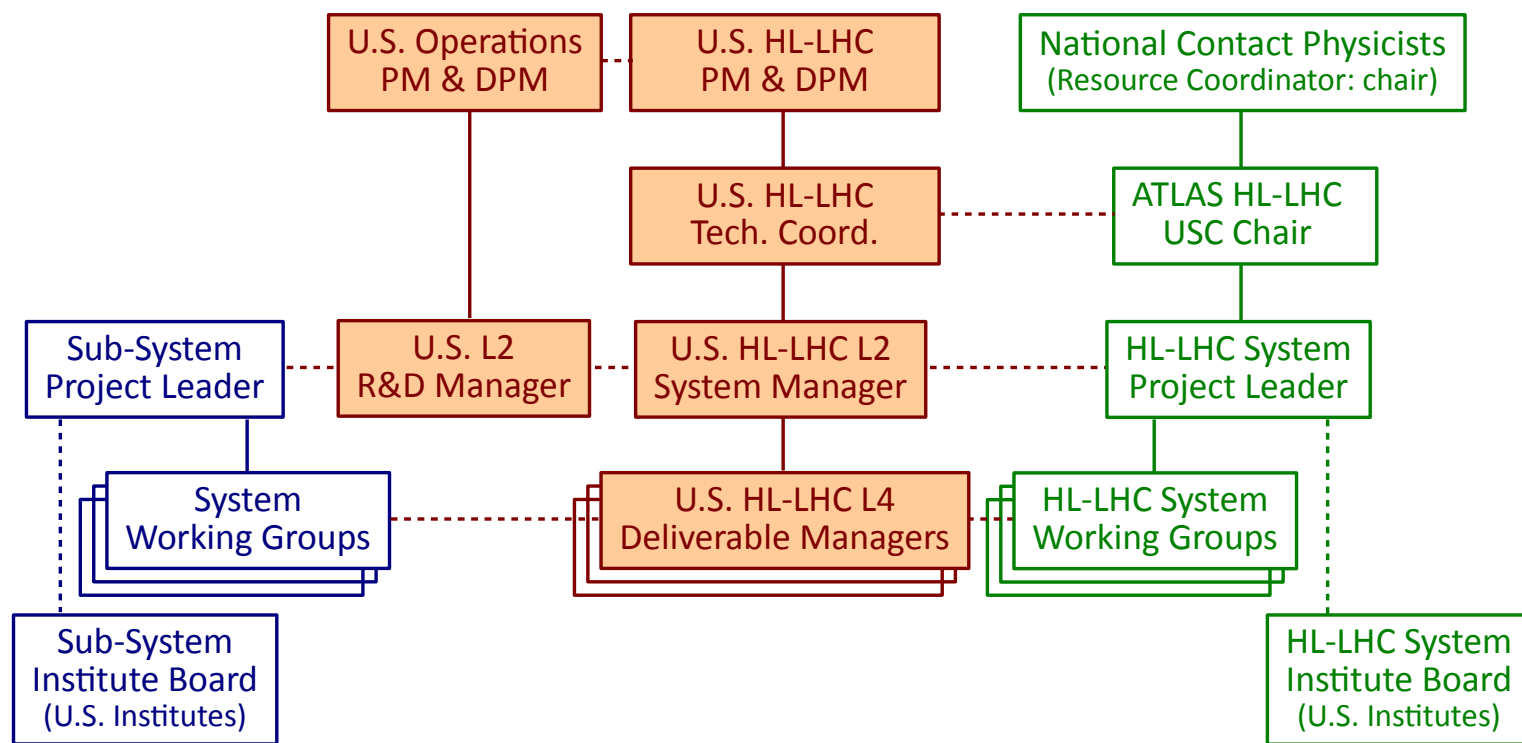


ATLAS Structure

ATLAS Operations

U.S. ATLAS

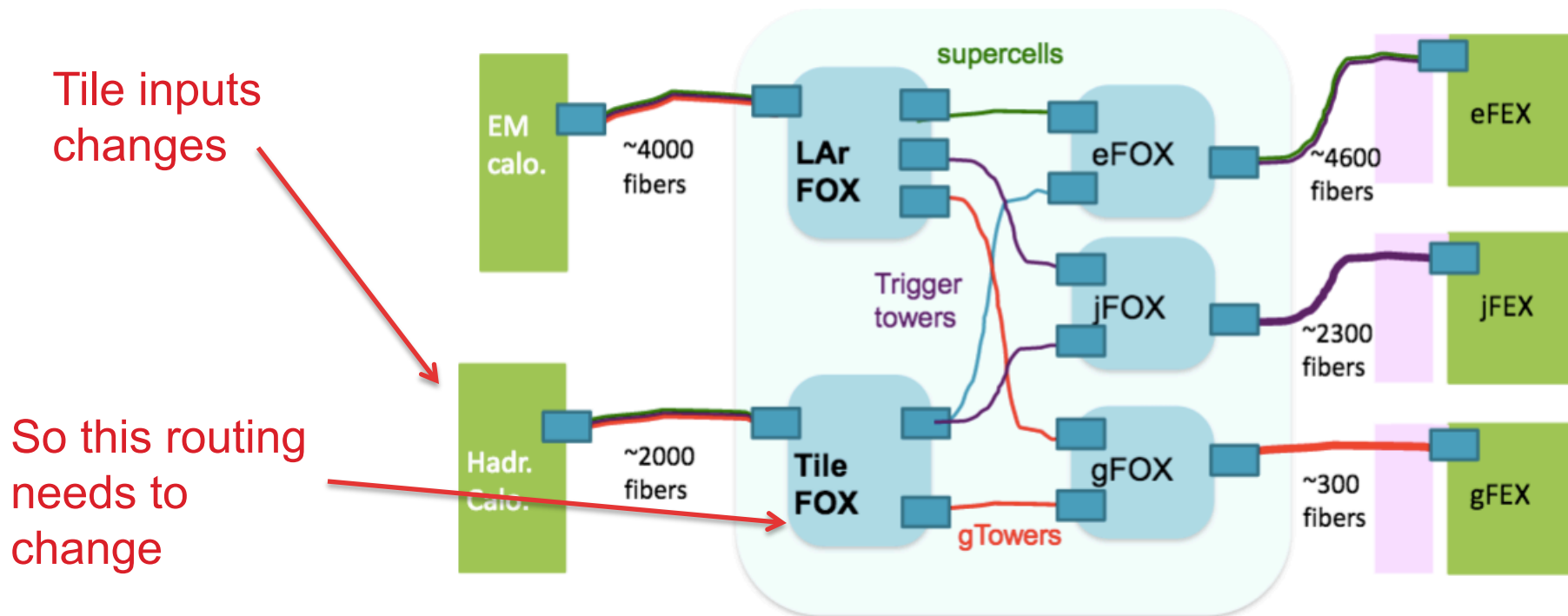
ATLAS HL-LHC





6.8.y.1: L0 Calo Fiber Optic Plant

- Rebuild the Phase-1 Fiber Optic plant to accommodate the change to the tile electronics
- Builds on unique MSU experience with fiber routing and splitting



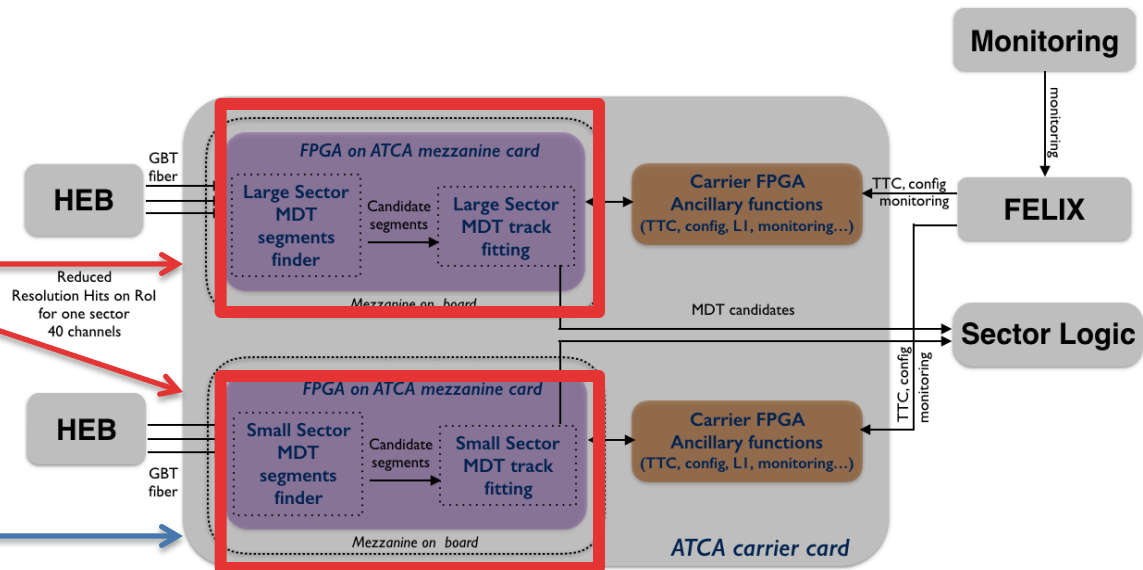


6.8.y.2: L0 Muon

- Deliverable is a mezzanine card with firmware that sits on a carrier card that handles the I/O with the system
 - Mezzanine find track segments, links them, and fits tracks
 - Contributes to muon rate reduction and efficiency improvement

These are the mezzanines

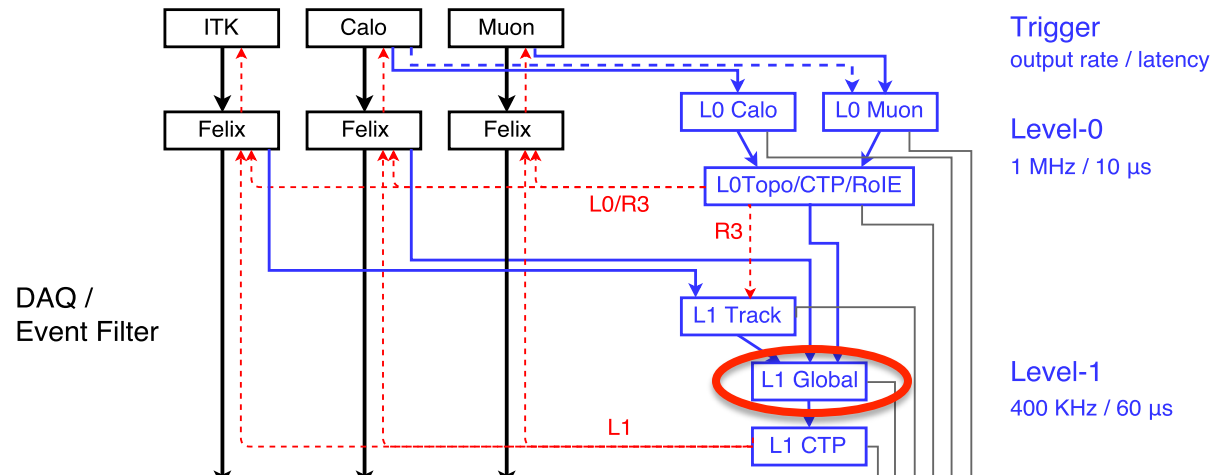
They sit on a carrier card (non-US) which handles data routing





6.8.y.3: L1 Global Processing

- Deliverable is firmware that runs on the L1 Global Processor
 - The focus is on hadronic triggering with 4 related items
 - Offline-like “topological clustering” of calorimeter energy
 - Offline-like jet finding
 - Global quantities: Missing energy, sum of jet pTs (HT), and MHT
 - Track-based pile-up rejection for multijet and global quantities
- Follows Phase-1 experience with the gFEX system
 - gFEX is global quantities and fat-jets at what will be L0 in HL-LHC





6.8.y.4: L1Track/FTK++ processing

- L1Track/FTK++
 - L1Track provides regional tracking at 1 MHz at low-latency as input to L1 Global
 - Many many uses... key for electron, tau, and multiobject hadronic triggers
 - FTK++ provides full detector tracking to be used in the Event Filter (PC farm)
 - This is expected to be critical for maintaining sharp turn-on curves for offline definitions of jets and MET than involve tracking
- The L1Track/FTK++ systems are expected to use the same hardware with minor modifications
- Each system consists of two stages:
 - pattern recognition step with a preliminary track fit
 - second track fitting stage to include additional hits not used in pattern recognition
- Both stages are expect to use the same mainboard for data preparation
- Each stage will have its own mezzanine
- Deliverables are
 - Mainboard design and firmware (50% of hardware)
 - 100% Second-stage hardware and firmware



Quality Assurance Plans

Definition of Successful End of Project

- 6.8.y.1 L0 Calo
 - Delivery of assembled and tested system
- 6.8.y.2 L0 Muon
 - Delivery to CERN of 32 AMCs which have been tested with the carrier boards
- 6.8.y.3 L1 Global Processing
 - Completion functional algorithms with adequate demonstrated performance, resource consumption and timing
- 6.8.y.4 L1Track/FTK++
 - Delivery of boards to CERN with firmware that is ready for an full integration test (slice test will be a year early)